SA-1500:
A 300 MHz RISC CPU with Attached Media Processor*

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*SA-1500 was designed by Digital Semiconductor’s Palo Alto Design Team.
Outline

- High Level Overview
- System Architecture
- SA-1500 Architecture
- Programming Model
- Companion Chip for Video
- Summary
High Level Overview

Design Goals

- High Performance for Multimedia Applications
- Flexible, General Purpose Architecture
- Easily Targeted for Different Market Segments
- Lower Cost for High Volume
- Low Power
# High Level Overview

## Specifications

<table>
<thead>
<tr>
<th>FEATURE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.28 micron CMOS</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>3.3 Million</td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>200-300 MHz</td>
</tr>
<tr>
<td>Die Size</td>
<td>$60 \text{ mm}^2$</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>$&lt;$ 0.5 W @ 100MHz</td>
</tr>
<tr>
<td></td>
<td>$&lt;$ 2.5 W @ 300MHz</td>
</tr>
<tr>
<td>Voltage</td>
<td>Internal: 1.5-2.0V</td>
</tr>
<tr>
<td></td>
<td>I/O: 3.3V</td>
</tr>
<tr>
<td>Packaging</td>
<td>240-pin MQFP</td>
</tr>
<tr>
<td></td>
<td>256-pin PBGA</td>
</tr>
<tr>
<td>Clocking</td>
<td>Dynamic clk freq. switching</td>
</tr>
</tbody>
</table>
High Level Overview

Performance Target

- Replace Microprocessor and DSP-HW in high-volume applications
- **Numeric and General-Purpose Processing**
  - Multimedia, DSP, and FP Applications
  - MPEG-2 MP@ML with power to spare
  - Modembank and multi-channel voice over IP
  - Video conferencing
- **Soft/scalable architecture**
- **High sustained memory bandwidth**
- **High multimedia code density**
- **Ease of programming**
High Level Overview

The System
High Level Overview

The System - Data Flow

SA1500
Computation Chip

IDE / PCMCIA

Bus I/F

ROM

DRAM

Network I/F

Video/Audio
Companion Chip

Video
Audio

SDRAM

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SA-1500 Architecture
Processor Block Diagram

- **Prefetch Buffer**: 256B
- **AMP**: Multimedia, DSP, and FPU Engines, 300MHz
- **Streaming Buffer**: 128B
- **StrongARM Execution Unit**: 300MHz
- **16KB DCache**: Mini DCache 1KB
- **16KB ICache**: 64-bit WCS 4KB
- **BIU**: Mem Ctrl/DMA
- **100MHz SDRAM Bus**: 100MHz
- **50MHz I/O Bus**: 50MHz

WCS = Writable Control Store

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SA-1500 CPU Attributes

- **Semi-autonomous dual-processor CPU**
  - Master-slave during invocation of AMP
  - Autonomous execution thereafter

- **Non-homogeneous instruction set**
  - 32-bit ARM instructions
  - 64-bit Long Instruction Word (LIW) AMP instructions (Arith || Mem/JMP)

- **Single-instruction Multiple-Data (SIMD) AMP Processing**
  - single-FMAC (32-bit), dual-IMAC (18-bit), quad-SAD (9-bit)

- **Memory Architecture**
  - Shared external memory
  - Shared Data Cache and Write Buffer
  - Separate Instruction Caches (Icache for ARM, WCS for AMP)
  - Separate Stream (pre-fetch) Buffers
SA-1500 Memory Controller and Bus Interface

- **100 MHz SDRAM Memory Controller (SBus):**
  - Programmable bus clock
  - 32-bit mode

- **50 MHz General I/O Bus (PBus):**
  - Programmable bus clock
  - Direct Connection to:
    - PC-style I/O devices
    - ROM/SRAM/DRAM/Flash
    - Bus adapter to PCI, PCMCIA

- **DMA controller with 15 descriptor-based channels**
AMP Block Diagram

FPU
Acc

MAC
Acc

ALU/Shift
Acc

64 GPRs

Ctl & Status Regs

Branch

Load/Store

Mem

WCS

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Processor Features

**StrongARM**
- 32 bit RISC, ARM V4 Architecture
- 16K Icache, 16K Dcache, Write buff
- High Code Density
- All Instructions Conditional
- Operand Shift Support for ALU Inst
- Powerful 32 x 32 + 64 -> 64 MAC

**AMP**
- Dual Issue instructions
  - 1x SIMD Arithmetic (ALU, MAC, FPU)
  - 1x Memory or Branch
- Dual personality
  - coprocessor or parallel processor
- Variety of Register DataTypes
  - 8/9b, 16/18b, 32/36b, 32-bit FP
  - 64 registers (36 bits wide)
- Fully Pipelined Operations
- 512-instruction WCS
AMP Operations

- Fully pipelined

**Arithmetic operations**

- ALU/MAC/FPU Operations:
  - 8b mul with scale/round/sat
  - 9b averaging, pack/unpack
  - 9/18b add, sub, motion estimation
  - 18/36b mul, mul-add, mul-sub with scale/round/sat
  - 32/36b add, sub, shift, logical
  - Single Precision FPU: mul-add, mul-sub, div, sqrt

- Fully pipelined

**Memory and Branch operations**

- Load/Store/Branch Operations:
  - Reg+Disp, Reg+Scaled-Index
  - Reverse-byte, replicate, texel loads
  - Transpose stores with auto-update
  - Single-inst compare and branches
  - Decrement and branch
SA-1500 Instruction Execution

- **Parallel Method**
  - StrongARM “library call” to WCS entry
  - USAGE:
    - MPEG-II Decoding
    - 3-D/Graphics Libraries
    - Application-Specific Functions

- **Tightly Coupled Method**
  - Issue an “Execute” or a “Memory/Branch” operation in StrongARM inst stream
  - Supported by the C compiler

### StrongARM AMP EXU AMP MBU

<table>
<thead>
<tr>
<th></th>
<th>AMP EXU</th>
<th>AMP MBU</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>3</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>4</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

- Supported by the C compiler.
SA-1500: Programming Flexibility

Multimedia Programming Model

- Media-Processor + Fast RISC Core
- Multimedia-Enhanced, Fast RISC Core
- Fast RISC Core

Performance vs. Programming Effort

- StrongARM native
- AMP: Tightly Coupled
- AMP: Parallel Method

AMP Asm Libraries
SA Asm Libraries
HLL Compiled Libraries

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Example of AMP Processing Flow

- **FIR Filtering:**
  \[ y(m) = \sum_{n=0}^{N-1} h(n) x(m-n), \quad m = 0, 1, \ldots, M - 1 \]

- **Assume:** 16-bit data & coeff, \( N = 64 \), \( M = \) multiple of 128, dual-MAC processing

- **AMP Processing:**
  - Prefetch data \( x[0:63] \) into PFB[0:63]
  - Load coefficients \( h[0:63] \) into registers L0-L31
  - Loop \( m=1:M/128 \)
    - Prefetch data \( x[m*64:m*64+63] \) into PFB[64:128]
    - Compute and store \( y[(m-1)*64: (m-1)*64+63] \)
    - Prefetch data \( x[(m+1)*64:(m+1)*64+63] \) into PFB[0:63]
    - Compute and store \( y[m*64: m*64+63] \)
  - Update FIR states \( x[0:63] \)
Multimedia Processing

- **MPEG-2 Decode**
  - Main Level/Main Profile: 720x480x30FPS
  - Processor Load Balancing:
    - *StrongARM*: All processing above MacroBlocks (coded in C)
    - *AMP*: MacroBlocks down (hand-coded)
  - Audio processing using FPU

- **Modembanks**
  - Can Support multiple modems (V.34 or V.90)

- **Video Conferencing**
  - H.324

- **Voice over IP**
  - Can support multiple digital voice channels (ITU G.72x plus echo cancellation)
Example Application: MPEG-2 decode

◆ **Transport Stream De-multiplex**
  - Companion chip: Filters transport stream
    - Adds timestamps for synchronization
    - Tags packets, DMA's into SDRAM
  - StrongARM: Splits stream into components

◆ **Audio Decoding:** Decodes MPEG 2 audio in software
  - StrongARM: Control, bitstream parsing, dequantize, float
  - AMP: IDCT, windowing, fix pt cvt, store
  - Companion chip: Formats, drives external DACs (x6)

◆ **Video Decoding:** Can decode full MPEG-2 MP@ML in software
  - StrongARM: Control, bitstream parsing, VLC decoding
  - AMP: Dequantize, IDCT, motion-reconstruction
  - Companion chip: Scaling, mixing with overlay data Pan & Scan
Companion Chip: Architecture

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Companion Chip: Video/Network

- **Flexible Network Interface w/ Packet Filtering**
  - up to 155 Mbit receive and transmit channels

- **ITU601 Digital Video Generation System**
  - Movie Stream and Palletized Graphics
  - Up/down horizontal scaling (320 tap filter)
  - Palletized Cursor/Pointer overlay
  - Variable mix of Movie and Graphics
  - On chip fully programmable pixel clock VCO/PLL

- **Digital Video Output**
  - NTSC, PAL encoding, or direct monitor drive
  - Macrovision (tm) Anti-taping Option
  - Composite, S-Video or RGB output
Companion Chip: Low Speed I/O

- **Serial Ports**
  - Up to 6 Channel Audio Output System
    - Serial Digital Output to External DACs
  - IrDA + Generic Infra-Red Interfaces
  - Telephone Quality CODEC Interface for Audio Input
  - PS/2 Keyboard/Mouse Interfaces
  - Smart Card Interface

- **IEEE1284 Parallel Port Interface**

- **General Purpose Timers**

- **Flexible Interrupt Controller**

- **General Purpose I/Os**