VelaTX™

Innovative 3D Architecture Coupled with Embedded DRAM Architecture

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Joseph C. Del Rio, V.P. Engineering
Problem Statement

- Traditional 3D graphic game engines architectures with external ram solutions cannot meet the increased demand for higher visual realism.
Traditional 3D Graphics Engine (T3D) Memory Storage Requirements

<table>
<thead>
<tr>
<th>Resolution</th>
<th>16-bit Z</th>
<th>24-bit Z</th>
<th>32-bit Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>640x480</td>
<td>2.9</td>
<td>3.5</td>
<td>4.1</td>
</tr>
<tr>
<td>800x600</td>
<td>4.6</td>
<td>5.5</td>
<td>6.4</td>
</tr>
<tr>
<td>1024x768</td>
<td>7.5</td>
<td>9.0</td>
<td>10.5</td>
</tr>
<tr>
<td>1280x1024</td>
<td>12.5</td>
<td>15.0</td>
<td>17.5</td>
</tr>
<tr>
<td>1600x1200</td>
<td>18.3</td>
<td>22.0</td>
<td>25.6</td>
</tr>
</tbody>
</table>

Note: No texture maps, polygon lists
T3D Memory Storage Requirements

At Even Higher Resolution….

24-bit RGB

<table>
<thead>
<tr>
<th>Resolution</th>
<th>16-bit Z</th>
<th>24-bit Z</th>
<th>32-bit Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>1024x768</td>
<td>7.5</td>
<td>9.0</td>
<td>10.5</td>
</tr>
<tr>
<td>1280x1024</td>
<td>12.5</td>
<td>15.0</td>
<td>17.5</td>
</tr>
<tr>
<td>1600x1200</td>
<td>18.3</td>
<td>22.0</td>
<td>25.6</td>
</tr>
<tr>
<td>2560x1920</td>
<td>46.9</td>
<td>56.3</td>
<td>65.6</td>
</tr>
</tbody>
</table>

Note: No texture maps, polygon lists
Traditional Frame Buffer access method

2 + 2 \times (1 + 0.5) = 5 \text{ accesses}

Depth complexity = 3

Each Pixel is Z compared and replaced if the test passes.
Number of per pixel access of Various Filters

\[(1+2(0.5)) \times \text{filter reads} = \text{total}\]

<table>
<thead>
<tr>
<th></th>
<th>point</th>
<th>bi-linear</th>
<th>tri-linear</th>
<th>anisotropic</th>
</tr>
</thead>
<tbody>
<tr>
<td>number of accesses</td>
<td>2.0</td>
<td>8.0</td>
<td>16.0</td>
<td>32.0</td>
</tr>
</tbody>
</table>
Summary of Bandwidth Requirements for T3D

Note: Trilinear Mipmapped, 24 bpp texel, 24-bits Z, 60 fps, Depth Complexity=3
T3D Transparency dither artifacts

T3D Image

Note dither pattern effect

VelaTX Image
Comparative memory transfer rates

![Graph showing comparative memory transfer rates for different memory types and frequencies. The x-axis represents the number of "In-Page" transfers, and the y-axis represents the bandwidth in M xfrs/s independent of bus width. The graph compares SD/SGRAM at 125MHz and 166MHz, and eMDRAM at 125MHz and 166MHz.]
Sustained Bandwidth Comparison for some implementations

- **SG/SDRAM 64-bit**: 166 MHz
- **SG/SDRAM 128-bit**: 166 MHz
- **eMDRAM 512-bit**: 125 MHz

Additional 266MB/s for 1024x768 72Hz integrated RAMDAC

A T3D 1024x768 24bpp x24bit Z x60fps at depth complexity 3 requirement

**Number of "In-Page" transfers**

**BW in Gbytes/s**
Texture look-ups at depth complexity of 3 for various levels of Transparency

Note: Assumes no game ordering of transparent polygons.
PixelSquirt™
Screen Order/Linear Frame Buffer Rendering
Pixel Squirt 3D core
Z Elimination savings over T3D Z storage

<table>
<thead>
<tr>
<th>Resolution</th>
<th>No Z</th>
<th>Z (T3D)</th>
</tr>
</thead>
<tbody>
<tr>
<td>640x480</td>
<td>1.2</td>
<td>2.9</td>
</tr>
<tr>
<td>800x600</td>
<td>1.8</td>
<td>4.6</td>
</tr>
<tr>
<td>1024x768</td>
<td>3.0</td>
<td>7.5</td>
</tr>
</tbody>
</table>

Note: 16 bits per pixel, 24 bit Z, double buffered
Z Elimination savings over T3D Z storage
(at even higher resolutions)

Note: 16 bits per pixel, 24 bit Z, double buffered
Note: Trilinear Mipmapped, 24 bpp texel, 24-bits Z, 60 fps, Depth Complexity=3, 50% translucency
Bandwidth Requirements to handle the Depth=20 “explosion” frame

<table>
<thead>
<tr>
<th>Resolution</th>
<th>T3 D</th>
<th>VelaTX</th>
</tr>
</thead>
<tbody>
<tr>
<td>640x480</td>
<td>5.44</td>
<td>1.58</td>
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<tr>
<td>800x600</td>
<td>8.50</td>
<td>2.47</td>
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<tr>
<td>1024x768</td>
<td>13.93</td>
<td>4.05</td>
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<tr>
<td>1280x1024</td>
<td>23.22</td>
<td>6.74</td>
</tr>
<tr>
<td>1600x1200</td>
<td>34.01</td>
<td>9.88</td>
</tr>
</tbody>
</table>

Note: Trilinear Mipmapped, 24 bpp texel, 24-bits Z, 60 fps, Depth Complexity=20, 50% translucency
VelaTX™ Internal Block Diagram

- PCI 66Mhz bridge
- P Pipe
- GPIO
- ClockGen
- Multi-client bus
- Target Bus control
- AGP 2X
- MasterReadBus
- 3D/2D Core
- PixelSquirt
- Command sequencer and DMA controller
- CRTC
- ramdac
- Unified Memory Controller
- Single 512 bit port
- eMDRAM block

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Summary

● 3D is fundamentally memory storage and bandwidth intensive
● T3Ds hit the wall at 1024x768, true color, 60FPS, and increasing depth complexity and texture filters.
● Attack the problem from both sides
  ● Pixelsquirt architecture eliminates the Z portion of the storage problem
  ● Pixelsquirt architecture reduces the texture bandwidth demand
  ● eMDRAM architecture increases the texture bandwidth supply