POWER4 Test Chip

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Presentation Overview

- Design objectives
- Chip overview
- Technology
- Circuits
- Implementation
- Results
Test Chip Objectives

Technology feasibility
- Understand product level Silicon technology
- Vehicle for small device level experiments from manufacturing as well as design
- Understand product level packaging technology

Critical circuit learning
- Logic circuitry
- Clocks
- I/O
- Arrays
- Power delivery

Design team skills building
- 40% of product design team contributed to the POWER4 test chip design
- Many facets of the design exercised to product level requirements

Tools learning
- > 80% of point tools exercised
- Execute methodology on a large chip
Test Chip Overview

Powered on 12/17/98

Included in POWER4 Test Chip:
- Experiments from each unit of the POWER4 chip (called DUTs)
- L1, L2, trace and SLB caches
- Product level pumped I/O design implemented
- Product level clock design implemented
- Experiments to stress power delivery
- Engineering and service processor interface
- On chip tester

Chip characteristics:
- 379 mm²
- 35 million transistors
- 2,217 chip signal I/Os

Built to product level test requirements
On chip tester
- 640 bit wide, 16 cycle deep vector generation and compare
- Vector ordering, selection, and loop control is programmable
- Cycle accurate result compare
- Random pattern generation mode with MISER

Noise generation
- Cycle by cycle programmable noise generation
- Chip contains 384 noise generation macro's
- Each macro noise amplitude and signature is programmable
- Each cycle noise generator macros can dissipate a total of 0 - 100W

Chip interface, debug infrastructure and test
- Chip accessed and programmed using product level support processor
- Manufacturing level test infrastructure implemented
- On-chip logic analyzer implemented for debug purposes
- Product level clock controls implemented
CMOS 8S Technology

- 0.18 micron general lithography
- Silicon on insulator substrate
- 7 layers of metal, all Cu
- SRAM cell size: 4.23 sq microns
- Vdd = 1.5V

Package Technology

- Glass substrate
- No thin film required
- > 5500 4mil C4 chip to substrate connections
- C4 connections on an 8mil pitch
Circuit design verification

Clocks
- High frequency PLL design compared to low jitter reference source
- On chip clock distribution latency and skew measured

I/O
- Elastic and non-elastic I/O implemented and measured
- Performance of both I/O types "chip" limited

Arrays
- L1, L2 and SLB implemented and measured
- The performance and density critical L2 cache design is solid

Power/Noise experiments
- Noise amplitude measured under several different current excitations
- Package impedance empirically determined for full GHz bandwidth
Clock source experiment

800 MHz Clock Jitter

- No Noise
- Noise Group 1
- Noise Group 2
- Noise Group 3

- CLOCK OUT W/BYPASS
- CLOCK OUT W/PLL
- REF CLK OUT W/BYPASS
Measured Clock Skew

IBM

70 ps skew (worst chip)
26 points probed
Test Chip contains product like I/O architecture

- Approximately 800 elastic I/O signals
- Approximately 1400 synchronous I/O

Elastic I/O performance

<table>
<thead>
<tr>
<th>Voltage</th>
<th>A5 Pattern</th>
<th>OF Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.3</td>
<td>462</td>
<td>453</td>
</tr>
<tr>
<td>1.4</td>
<td>459</td>
<td>450</td>
</tr>
<tr>
<td>1.5</td>
<td>462</td>
<td>465</td>
</tr>
<tr>
<td>1.6</td>
<td>462</td>
<td>468</td>
</tr>
<tr>
<td>1.7</td>
<td>465</td>
<td>453</td>
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</tbody>
</table>

Synchronous I/O performance

<table>
<thead>
<tr>
<th>Voltage</th>
<th>No Noise</th>
<th>FFFFFFFF</th>
<th>FFFFF0000</th>
<th>F00000000</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.3</td>
<td>978</td>
<td>906</td>
<td>810</td>
<td>816</td>
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<tr>
<td>1.5</td>
<td>1098</td>
<td>1002</td>
<td>912</td>
<td>954</td>
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<tr>
<td>1.7</td>
<td>1128</td>
<td>1026</td>
<td>978</td>
<td>1032</td>
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</tbody>
</table>
**L2 Cache Test Results**

**L2 cache macro:**
- 2 cycle access latency
- Row and column redundancy
- Array efficiency > 75%
- Includes ABIST

<table>
<thead>
<tr>
<th>Wafer/Chip</th>
<th>MAX ABIST FREQ (MHz)</th>
<th>VDD (V)</th>
<th>CHUCK TEMP (deg C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FY/4,7</td>
<td>1430</td>
<td>1.4</td>
<td>25</td>
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<tr>
<td>FY/7,7</td>
<td>1360</td>
<td>1.4</td>
<td>25</td>
</tr>
<tr>
<td>FY/7,4</td>
<td>1420</td>
<td>1.4</td>
<td>25</td>
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<tr>
<td>PY/5,4</td>
<td>1500</td>
<td>1.5</td>
<td>40</td>
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</tbody>
</table>
Measured Noise Results - Time Domain

**FFFF0000_all - PLL**

- 4 IDC 16 c4 cap
- No IDC 1 c4 cap
- No IDC 16 c4 cap
- No IDC No c4 cap
- No IDC 8 c4 cap

**FFFFFFF_all - PLL**

- 4 IDC 16 c4 cap
- No IDC 8 c4 cap
- No IDC 16 c4 cap
- No IDC 1 c4 cap
- No IDC No c4 cap

IBM
Measured Noise Results - Freq. Domain

IBM

Impedance vs Frequency

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<table>
<thead>
<tr>
<th>Frequency</th>
<th>Impedance</th>
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<tbody>
<tr>
<td>0</td>
<td>0.1</td>
</tr>
<tr>
<td>100</td>
<td>0.2</td>
</tr>
<tr>
<td>225</td>
<td>0.3</td>
</tr>
<tr>
<td>350</td>
<td>0.4</td>
</tr>
<tr>
<td>425</td>
<td>0.5</td>
</tr>
<tr>
<td>512.5</td>
<td>0.6</td>
</tr>
<tr>
<td>587.5</td>
<td>0.7</td>
</tr>
<tr>
<td>650</td>
<td>0.8</td>
</tr>
<tr>
<td>775</td>
<td>0.9</td>
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<tr>
<td>862.5</td>
<td>1.0</td>
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<tr>
<td>975</td>
<td>1.0</td>
</tr>
<tr>
<td>1100</td>
<td>1.0</td>
</tr>
</tbody>
</table>
```

- 4 IDC 16 c4 Caps
- No IDC, C4 caps
Voltage Schmoo

1.12 V 1.3 V 1.5 V 1.6 V 1.8 V 2.0 V 2.2 V

ecc  fxu200  idu
ifu301  slb1  fpumax
ifur1  wire
isu2
We have demonstrated that the POWER4 Clock, I/O, array and power delivery designs support GHz operation.

Significant portions of the POWER4 product design have been implemented and tested.

The POWER4 service processor interface, manufacturing test and debug design has been implemented and tested.

The POWER4 design team has built a product like chip utilizing the product design tools and methodology.