TM-1300 High-speed, Low-cost, Enhanced PCI, VLIW Media Processor

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Content

• Highlights
• Enhanced very-long instruction word (VLIW) engine
• System-on-a-chip
• Silicon information
• Conclusion
TM-1300 Applications

- Standalone or PC-based systems
- Video editing
- Videoconferencing (including modem)
- Security systems
- Digital television
- Set-top decoder/web browser
- DVD decoder
- Audio/Video en/de/transcode (Dolby AC-3®, MPEG)
**TM-1300 Block Diagram**

**System-on-a-chip**

- **CCIR601/656 YUV 4:2:2**
  - up to 80 MHz (40 Mpix/sec)

- **Stereo digital audio**
  - I²S - up to 20 MHz

- **Huffman decoder**
  - Slice-at-a-time MPEG-1 & -2

- **32-bit data**
  - 572 MB/sec BW

- **VIDEO IN**
  - CCIR601/656 YUV 4:2:2 up to 80 MHz (40 Mpix/sec.)
  - 2/4/6/8 ch. digital audio I²S - up to 20 MHz

- **VIDEO OUT**
  - IEC958, up to 40 mbit/sec
  - to V.34 or ISDN front end

- **AUDIO IN**
  - I²C bus to camera, etc.

- **AUDIO OUT**
  - Down & up scaling YUV to RGB 50 Mpix/sec

- **SPDIF OUT**
  - PCI/XIO (32 bits, 33 MHz)
  - 24 address bit, 8-bit data

- **TIMERS**
  - VLIW CPU
  - INSTR CACHE
  - DATA CACHE

- **DVDD**

- **VLD COPROCESSOR**

- **SYNCHRONOUS SERIAL INTERFACE**

- **I²C INTERFACE**

- **IMAGE COPROCESSOR**

- **PCI/XIO INTERFACE**

**Let's make things better**

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TM-1300 System Software Support

- Powerful C/C++ compiler
  - interprocedural analysis
  - automated in-lining, unrolling
  - shows an increase in performances up to 15%
- No assembly programming required
- pSOS+™ embedded, real-time kernels
  - code size: 130 KB
  - overhead: 5-10%
- Multiprocessor run-time and multitasking debug support
- Extensive multimedia library including several real-time video decompression standard packages
TM-1300 VLIW Highlights

- Instruction cache
  - 32-KB, 64-byte block size
  - 8-way set associative
  - contains compressed VLIW instructions
- Dual-ported data cache
  - 16-KB, 64-byte block size
  - 8-way set associative
- Up to 5 RISC operations per cycle
- Conditionally guarded operations
- Multimedia operation set (extended for median filter and 9-bit iDCT support)
Median Filter

Used to De-Interlace a CCIR601 Resolution Video

\[\begin{align*}
IN1 & \leq IN2 \leq IN3 \\
IN3 & \leq IN2 \leq IN1 \\
IN1 & \leq IN3 \leq IN2 \\
IN2 & \leq IN3 \leq IN1
\end{align*}\]

- \(\text{OUT} = \text{IN2}\) if \(\text{IN1} \leq \text{IN2} \leq \text{IN3}\)
- \(\text{OUT} = \text{IN1}\) if \(\text{IN3} \leq \text{IN2} \leq \text{IN1}\)
- \(\text{OUT} = \text{IN3}\) if \(\text{IN1} \leq \text{IN3} \leq \text{IN2}\)
- \(\text{OUT} = \text{IN2}\) if \(\text{IN2} \leq \text{IN3} \leq \text{IN1}\)

Median Filter
Median Filter

- \( R_0 = \text{QUADUMIN}(\text{IN1}, \text{IN2}) \)
- \( R_1 = \text{QUADUMAX}(\text{IN1}, \text{IN2}) \)
- \( R_2 = \text{QUADUMAX}(R_0, \text{IN3}) \)
- \( \text{MEDIAN}(\text{IN1}, \text{IN2}, \text{IN3}) = \text{QUADUMIN}(R_1, R_2) \)
Performance Improvement

- Original TM-1000 requires 35 operations for 4 pixels; TM-1300 requires only 8 operations
- Reduces CPU load from 63% to 29% for the full application with only two new operations
- Similarly 9-bit precise iDCT has been improved by 11% using 4 new operations dualasr, dualiclipi, dualuclipli, mergedual16lsb
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VIDEO IN
AUDIO IN
TIMERS
DVDD
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VLIW CPU

VIDEO OUT
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I²C INTERFACE
IMAGE COPROCESSOR
PCI/XIO INTERFACE

32-bit data 572 MB/sec BW
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INTERNAL BUS (DATA HIGHWAY)
Arbiter Characteristics

- Round robin
- Programmable
- Hierarchical
- Low- and high-priority requests
Arbiter Block Diagram

L1 arbitration
1/2/3

L2 arbitration
1/3/5
1/3/5/7

L3 arbitration
1/3/5/7
1/3/5

L4 arbitration
1/2
1/3/5

L5 arbitration
1/3/5
1/2

L6 arbitration
2
1
1
1
1
1

cache priority-based arbitration

ic_req
dc_mmio_req
dc_mmio_req

vo_req
icp_req
vi_req

pci_req
pci_mmio_req

vld_req
ao_req
ai_req
spdio_req
dvdd_req

Let's make things better
Arbiter Implementation

For CPU weight of 3 and L2 weight of 1, states used are 0, 2, 4 and 1
**Arbiter: Latency**

\[ L_i = (D_i \times T) + E + \text{REF} + \text{LOW} \]

- \( T = 20 \) SDRAM cycles (transaction length)
- \( E = 10 \) SDRAM cycles (critical word first)
- \( \text{REF} = 19 \) SDRAM cycles (SDRAM refresh)
- \( \text{LOW} = \) the number of cycles the request is at low priority

\[ D_{\text{CPU}} = \text{ceil} \left( \frac{\text{CPU}_{\text{weight}} + \text{L2}_{\text{weight}}}{\text{CPU}_{\text{weight}}} \right) \]

\[ D_{\text{VO}} = \text{ceil} \left( \frac{\text{VO}_{\text{weight}} + \text{L3}_{\text{weight}}}{\text{VO}_{\text{weight}}} \right) \times D_2 + 1 \]

\[ D_2 = \text{ceil} \left( \frac{\text{CPU}_{\text{weight}} + \text{L2}_{\text{weight}}}{\text{L2}_{\text{weight}}} \right) \]
Arbiter: Bandwidth

\[ B_i = \frac{(Mcycles - K) \times 64}{(E_i \times T)} \]

\( T \) = 20 SDRAM cycles (transaction length)
\( K \) = the number of cycles taken by the refresh over the period \( Mcycles \)

\[
E_{CPU} = \left( \frac{CPU_{weight} + L2_{weight}}{CPU_{weight}} \right)
\]

\[
E_{VO} = \left( \frac{VO_{weight} + L3_{weight}}{VO_{weight}} \right) \times E_2
\]

\[
E_2 = \left( \frac{CPU_{weight} + L2_{weight}}{L2_{weight}} \right)
\]
High-Speed SDRAM Interface

- Up to 64 MBytes
- 64 Mbit generation organized in x32 and x16
- Up to 143 MHz with 4 chips load (32 MBytes)
- Expected to support 166 MHz
- Sustains full bandwidth thanks to pipelined and optimized SDRAM accesses:
  - Interleaved bank access every 32-byte block
MPEG-2 Performance

- 180 MHz CPU speed and 143-MHz SDRAMs
- For high-action DVDs, such as *Twister*, *The Mask* or *Star Ship Troopers*
TM-1300 Silicon

- 58 mm²
- 6 metal layer
- 5.6 million of transistors
- .25 µm, 2.5 V core supply, 3.3 V I/O supply (5 V tolerant)
- 143 and 166 MHz at min. voltage (2.375 V) and 85 °C
- 180 to 200 MHz under more controlled conditions
- 3.2 W consumption for typical conditions
- Block level powerdown saves up to .5 W
- BGA292 (169 functional I/Os)
In Conclusion

- Powerful VLIW engine (average of 4 instructions/cycle)
- Low cost thanks to an integrated system-on-a-chip
- Excellent audio/video quality at low cost at system level
- For peak performances required by DVD playback: 180-MHz CPU with 143 MHz SDRAM