The Au1000™ Internet Edge Processor: A High Performance, Low Power SOC

The First Chip in a Family of Parts from Alchemy Semiconductor, Inc.

Suzanne Plummer

Hot Chips 2000
Agenda

- Design Goals
- High Performance Microarchitecture Highlights
- Low Power Microarchitecture Enhancements
- System Bus Structure / Coherency
- Peripherals / Integration Strategy
- Summary
Design Goals

- Design Goal: Highest Performance at .5W
- Design Goal: Industry Standard Architecture
  - MIPS Architecture License
  - Developed own microarchitecture and implementation
  - First in a family of parts
- Design Goal: Low Cost Production
  - Custom Core
  - Custom Cell Libraries for Synthesis
  - Portable Design and Layout Rule Set
  - Au1000 produced in standard TSMC .18µ LV Process
- Design Goal: Time to Market
  - Purchased IP Blocks
  - Optimal Circuit Design for time to market
Au1000 SOC

- LCD Controller
- PCMCIA
- Flash
- SRAM
- ROM
- X-Bus

SDRAM Controller
- Enhanced MIPS32 CPU
- IMMU
- Bus Unit
- 16KB I-Cache
- 16KB D-Cache

SRAM Controller
- System Bus
- Peripheral BUS IF
- RTC (2)
- Power Mgmt
- SSP
- SPI
- AC97 Link

Peripheral Bus
- Fast IRDA
- EJTAG
- DMA Controller
- Ethernet MAC
- Ethernet MAC
- USB – Host
- USB-Device
- Interrupt Control
- GPIO (6-32)
- I2S
- UART (4)
AU1000 ISA & Privileged Instructions

- Compliant with the MIPS32 standard
- MIPS II  R3000 integer instructions
- New Instructions
  - Multiply-add and Multiply subtract
  - Targeted multiply
  - Count Leading Zeroes/Count Leading Ones
  - Wait
  - Conditional move
  - Prefetch
- R4000 MMU and Privileged Architecture
**Au1 Core 5-Stage Pipeline**

<table>
<thead>
<tr>
<th></th>
<th>Fetch</th>
<th>Issue</th>
<th>Execute</th>
<th>Cache</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ALU</strong></td>
<td>I$  Reg Decode</td>
<td>Reg File Read</td>
<td>ALU</td>
<td>BUF</td>
<td>Reg File Write</td>
</tr>
<tr>
<td><strong>MEM</strong></td>
<td>I$  Reg Decode</td>
<td>Reg File Read</td>
<td>Fast Disp Add</td>
<td>TLB Tag Access</td>
<td>D$ Data Access</td>
</tr>
</tbody>
</table>

- Pipelined register file access into fetch stage
- Load/Store Effective Addr computed in I-stage
  - Gives cache two cycle access
### Au1 Core Load Pipeline Example

<table>
<thead>
<tr>
<th>Fetch</th>
<th>Issue</th>
<th>Execute</th>
<th>Cache</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fetch</td>
<td>Issue</td>
<td>Fast Disp Add</td>
<td>TLB</td>
<td></td>
</tr>
<tr>
<td>LUI</td>
<td>imm</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**LUI** \( r1, \) \( \text{imm} \)

**LW** \( rt, \) \( \text{offset} \) \( (r1) \)
Zero Penalty Branch

<table>
<thead>
<tr>
<th>Fetch</th>
<th>Issue</th>
<th>Execute</th>
<th>Cache</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADD R3,</strong> Fetch</td>
<td>Issue</td>
<td>Execute</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>BEQ R3,</strong> Fetch</td>
<td>Issue</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ADD</strong> Delay Slot Fetch</td>
<td>Fetch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>LW</strong> Fetch</td>
<td>Branch Target</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
High Performance MicroArchitecture Highlights

- Caches
  - 16K, Four-Way Set Associative Non-Blocking Data Cache
  - 16K, Four-Way Set Associative Instruction Cache
  - Write-back Cache
  - Allocate on Reads
  - Cache Line Locking Support
  - 32 Byte Line Size
  - Physically Tagged
  - Hit-under-miss in Data Cache
High Performance MicroArchitecture Highlights

- **Cache Management Features**
  - Programable Set Allocation Policy controlled by Page attribute
  - Line Locking
  - Prefetch Instructions (Instruction and Data)
- **Low Latency Access to on-chip buses**
- **Cache Coherency**
  - Coherent DMA support
  - Snooping for MP support
  - MESI protocol implemented
High Performance MicroArchitecture Highlights

◆ MMU
  – Hardware support for Software Breakpoints
  – Separate Interrupt Exception Vector
  – TLB
    ♦ 32 dual-entry fully associative
    ♦ Variable page sizes 4KB - 16MB
    ♦ 4 Entry ITLB

◆ Write Buffer
  – 16, 32-bit entries
  – Byte Merging and Word Gathering
High Performance MicroArchitecture Highlights

◆ Multiply-Accumulate (MAC) Hardware
  – One 32x16 MAC per Clock
  – One 32x32 MAC per Every Other Clock

◆ EJTAG
  – CPU Control with Start, Stop and Single stepping
  – Software Breakpoints via the SDBBP Instruction
  – Test Access Port Facilitates Download of Application Code
Low Power Microarchitecture Enhancements

- Aggressive use of Conditional Clocking
- 4-way associative data cache without requiring 4 data accesses
- No Speculative Execution
- Full speed Branches without Prediction
Low Power Microarchitecture Enhancements

- Pseudo-static design to 0 Hz
- Low Power modes
  - Idle1 – Clocks turned on to snoop system bus
  - Idle2 – Clocks not turned on for snoops
  - Sleep – Power down core
- Minimize Leakage with low power cell libraries
- Minimum VDDi at 1 V (approx)
- 3.3V I/O
# Power Estimates

<table>
<thead>
<tr>
<th>Power Mode</th>
<th>Operating Conditions</th>
<th>Estimated Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>1.25V, 200MHz</td>
<td>&lt;200mW</td>
</tr>
<tr>
<td></td>
<td>1.5V, 400MHz</td>
<td>500mW</td>
</tr>
<tr>
<td></td>
<td>1.8V, 500MHz</td>
<td>900mW</td>
</tr>
</tbody>
</table>
Au1 Core + System Bus

LCD Controller
PCMCIA
Flash
SRAM
ROM
X - Bus

SDRAM Controller

Peripheral BUS IF
RTC (2)
Power Mgmt
SSP
SPI
AC97 Link

System Bus

SDRAM

Fast IRDA
EJTAG
DMA Controller
Ethernet MAC
Ethernet MAC
USB – Host

Peripheral Bus
USB-Device
Interrupt Control
GPIO (6-32)
I2S
UART (4)
Alchemy System Bus

- 36-bit address bus
  - Additional address space to support bridges to external buses
- Connect through defined transceiver interface
- Bus clock ratios from 1/2 to 1/5 of core frequency.
Alchemy System Bus - Coherency

- Coherency Options
  - Nothing — force software to handle
  - Retry and push out to slow memory and re-read
  - Intervention — fastest device supplies data

- Alchemy System Bus Coherency Support
  - Intervention policy for high performance sharing
  - Supports multiple CPUs
  - DMA needs no extra logic to participate in data sharing
Intervention

DMAX/I/O Device

CPU

Memory

Read request

Supply data

Intervention reply

Line in memory not updated
Au1000 SDRAM Controller

- Tightly coupled SDRAM interface
  - Supports System Bus intervention protocol
- 32-bit interface
- 100 MHz SDRAM
- 3 software configurable chip selects allowing contiguous memory with different sizes and no adders
- ½ speed of system bus
- Low Latency SDRAM access
- Four open banks per chip select
Au1000 Static Controller

- Supports SRAM, Flash, ROM, and Page Mode ROM
  - Supports System Bus intervention protocol
- Supports 32- and 16-bit devices
- 4 chip selects
- Address and data lines can be used to control PC Card/Compact Flash, LCD, and external bus interfaces
Au1000 System Bus Peripherals

◆ USB Host Controller
  – Compliant with USB Protocol Revision 1.1
  – OHCI 1.0 Compliant

◆ DMA
  – 8 channel general purpose DMA controller for simple serial line support

◆ IrDA
  – Supports DMA, transmit and receive FIFOs, CRC and PHY layer
  – 4 Mb/sec

◆ Ethernet
  – 2 x 10/100 Ethernet MAC devices
  – Dedicated DMA controller
  – IEEE 802.3, 802.3u, 803.3x spec compliance
  – Full and Half duplex
Au1000 SOC

LCD Controller
PCMCIA
Flash
SRAM
ROM
X - Bus

SDRAM Controller

Enhanced MIPS32 CPU

DMMU

32 x 16 MAC

DMMU

16KB D-Cache

SDRAM

System Bus

Peripheral BUS IF

RTC (2)

Power Mgmt

SSP

SPI

AC97 Link

Fast IRDA

EJTAG

DMA Controller

Ethernet MAC

Ethernet MAC

USB – Host

USB-Device

Interrupt Control

GPIO (6-32)

I2S

UART (4)
Au1000 Peripheral Bus

- Peripheral Bus
  - Low latency access to simple peripherals
  - Allows I/O system access times to scale with CPU speed
  - Connect through defined transceiver interface
Au1000 Simple Peripherals

- **Interrupt Controller**
  - 2 interrupt controllers each supporting 32 interrupt sources
  - WAKEUP or CPU Interrupt

- **USB Device Controller**
  - Compliant with USB Protocol Revision 1.1

- **GPIO**
  - 2 x 32 port GPIO devices
  - 32 maximum
    - 6 dedicated pins
    - 26 shared pins
Au1000 Simple Peripherals

- **UART**
  - 4 UARTs
  - One UART supports modem Controls
- **SPI / SSP Serial Interfaces**
  - Two Additional for either SPI or SSP support
- **I2S Controller**
  - 3 or 4 line serial interface to Audio Codec
  - Philips spec compliant
- **AC97 Controller**
  - 4 line serial interface to AC97 Codec
Summary

- High Performance
  - 2X more performance than synthesized designs
  - 18 to 24 month time to market advantage in performance

- Low Power — Longer Battery Life
  - 3 – 5X more power efficient
  - 10X better standby efficiency: Designed for low leakage

- Integration — Lower System Cost
  - “Cut and paste” chip layout