Crusoe Power Management:

Cutting x86 Operating Power
Through LongRun

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Director, Low Power Programs
Transmeta Corporation

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Overview

🔗 Key Challenges for Mobile Computing
- "Portability" (weight) and "Ease of Use" (battery life)
- Power consumption is the key limiting factor

🔗 Solution - Crusoe Processor
- Full compatibility with x86 power management model
- Significantly lower power

🔗 LongRun
- Transmeta’s new invention to drive power savings
  - Adaptive Power Control (performance on demand)
  - Advanced Thermal Control (thermal budget expansion)
Power Density
The Fundamental Problem

Not too long to reach
Nuclear Reactor

Surpassed
Hot Plate

Pentium III®
Pentium II®
Pentium Pro®
Pentium®
i386
i486

W/cm²

1000
100
10
1

“Time”

Source: Fred Pollack, Intel. New Microprocessor Challenges in the Coming Generations of CMOS Technologies, Micro32
# X86 Power Management States

## A Quick Primer

<table>
<thead>
<tr>
<th>State</th>
<th>Description</th>
<th>Mobile x86 Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal (C0)</td>
<td>The CPU is actively executing instructions.</td>
<td>14.0 / 8.0</td>
</tr>
<tr>
<td>AutoHALT (C1)</td>
<td>CPU executes a low power instruction (x86: HLT).</td>
<td>1.7 / 1.1</td>
</tr>
</tbody>
</table>
| Quick Start (C2)| - CPU kills internal clocks (driven by South Bridge via STPCLK#).  
|              | - CPU maintains cache coherence (caches must be snooping).                | 1.3 / 0.8           |
| Deep Sleep (C3)| - South Bridge kills external clock input to the CPU.           
|              | - Maximum power savings w/o losing CPU context.                           
|              | - System enforces cache coherence (caches don’t need to snoop).          | 0.5 / 0.3           |

**ACPI Definition**
Advanced Communication and Power Interface Specification

**Mobile x86 Solution**
Processor
- 650 / 500 MHz
- 1.6 / 1.35 V
The Solution - Increase Efficiency

\[ P_{\text{ower}} = C_{\text{apacitance}} \times V_{\text{oltage}}^2 \times F_{\text{requency}} \]

- Transmeta Innovation - Code Morphing Software (CMS)
- Effect - Replace Millions of Logic Transistors with Software
  - … and transistors translate into capacitance
- Benefit - Significantly Reduces Power Consumption of x86 Power States
LongRun Adaptive Power Control
Maximize Battery Life With Performance on Demand

\[ \text{Power} = c \times v^2 \times f \]

- Dynamically adapt both frequency and voltage to performance demands
- Mechanisms in hardware
  - Fully programmable
- Policies in CMS
  - Adapt \( f \) to demand
  - Reduce \( v \) proportionally
  - Cubic power savings!

\[
\begin{array}{ccccccccc}
\text{Normal} & 12.5\% & 25.0\% & 37.5\% & 50.0\% & 62.5\% & 75.0\% & 87.5\% \\
\hline
\text{SDR} & 0.5 & 0.4 & 0.4 & 0.3 & 0.2 & 0.2 & 0.2 \\
\text{DDR} & 0.5 & 0.4 & 0.4 & 0.3 & 0.3 & 0.3 & 0.3 \\
\text{Core+NB} & 5.5 & 3.8 & 2.3 & 1.7 & 1.3 & 1.0 & 1.0 \\
\end{array}
\]

Cubic: Core + Northbridge
Linear: I/O (DDR, SDRAM)

- 133 MHz, 3.3 V
- 125 MHz, 2.5 V
- 633 MHz, 1.6 V
LongRun Adaptive Power Control vs. Traditional Power Management

<table>
<thead>
<tr>
<th>Idle Time</th>
<th>Normal</th>
<th>12.5%</th>
<th>25.0%</th>
<th>37.5%</th>
<th>50.0%</th>
<th>62.5%</th>
<th>75.0%</th>
<th>87.5%</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>LongRun</td>
<td>6.0</td>
<td>4.2</td>
<td>2.7</td>
<td>2.0</td>
<td>1.6</td>
<td>1.4</td>
<td>1.4</td>
<td>1.4</td>
<td>1.4</td>
</tr>
<tr>
<td>C3</td>
<td>6.0</td>
<td>5.3</td>
<td>4.5</td>
<td>3.8</td>
<td>3.0</td>
<td>2.3</td>
<td>1.5</td>
<td>0.8</td>
<td>0.0</td>
</tr>
</tbody>
</table>

Notes
1. Power numbers include Northbridge
2. DDR-only configuration

12th Hot Chips Symposium - August 15, 2000
LongRun Adaptive Power Control
Crusoe Power Profile

<table>
<thead>
<tr>
<th>Idle Time</th>
<th>Normal</th>
<th>12.5%</th>
<th>25.0%</th>
<th>37.5%</th>
<th>50.0%</th>
<th>62.5%</th>
<th>75.0%</th>
<th>87.5%</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power [W]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TM5400</td>
<td>6.0</td>
<td>4.2</td>
<td>2.7</td>
<td>2.0</td>
<td>1.6</td>
<td>1.2</td>
<td>0.8</td>
<td>0.4</td>
<td>0.0</td>
</tr>
</tbody>
</table>

Notes
1. Power numbers include Northbridge
2. DDR-only configuration

12th Hot Chips Symposium - August 15, 2000
The LongRun Effect
Power Profiles

<table>
<thead>
<tr>
<th></th>
<th>A/C</th>
<th>Conventional</th>
<th>Mobile x86</th>
<th>Multimedia (DVD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>650 MHz, 1.6 V</td>
<td>500 MHz, 1.3 V</td>
<td>633 MHz, 1.6 V</td>
<td></td>
</tr>
<tr>
<td>Battery</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power Profiles</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The LongRun Effect</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[W]</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Normal</th>
<th>12.5%</th>
<th>25.0%</th>
<th>37.5%</th>
<th>50.0%</th>
<th>62.5%</th>
<th>75.0%</th>
<th>87.5%</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>TM5400+NB</td>
<td>6.0</td>
<td>4.2</td>
<td>2.7</td>
<td>2.0</td>
<td>1.6</td>
<td>1.2</td>
<td>0.8</td>
<td>0.4</td>
<td>0.0</td>
</tr>
<tr>
<td>A/C</td>
<td>16.0</td>
<td>14.2</td>
<td>12.4</td>
<td>10.6</td>
<td>8.8</td>
<td>6.9</td>
<td>5.1</td>
<td>3.3</td>
<td>1.5</td>
</tr>
<tr>
<td>Battery</td>
<td>16.0</td>
<td>14.2</td>
<td>12.4</td>
<td>10.6</td>
<td>8.8</td>
<td>6.9</td>
<td>5.1</td>
<td>3.3</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Notes
1 Power numbers include Northbridge
2 DDR-only configuration
System Architecture

**Standard Applications**
No changes required

**Standard Operating System**
No changes required

**Standard BIOS**
No changes required

**Crusoe TM5400 processor featuring Transmeta LongRun technology**
Code Morphing software monitors system activity and dynamically adapts LongRun performance levels
Performance on Demand
Duty Cycle  Effective Performance Level

Performance

630 MHz
330 MHz
Sleep

Power

6.0 W
1.5 W
50mW
40mW

LongRun:
< 50% frequency reduction

50% duty cycle
Residual Sleep states

LongRun:
> 50% power reduction

Normal Sleep

LongRun: Low voltage Sleep
Transition Dynamics
Fast Frequency/Voltage Scaling

Pseudo Deep Sleep: < 20 µs

~ 20 µs per step

1.5 V

1.3 V

0 µs

100 µs

Frequency

Voltage

Time

CMS/LongRun policy decision

LongRun scales voltage asynchronously
Stepping: > 1.3 V: 50mV, < 1.3 V: 25 mV; max. ramping time: < 300 µs (1.6V to 1.1V)

Crusoe resumes x86 execution

LongRun trips clock change

Fast Frequency/Voltage Scaling
Transition Details
Voltage Scaling

- TM5400 Core Voltage is Fully Under Software Control
  - CMS directly controls voltage regulator pins (via internal processor register)
  - OEM configurable
    - CPU output pin/voltage mapping
    - Voltage settling interval
- CMS Schedules Interrupts to Asynchronously Ramp Voltage
  - Allows sustained x86 forward progress during voltage ramping
Transition Details
Frequency Scaling - Establish/commit control

<table>
<thead>
<tr>
<th>Clock Control</th>
<th>Shadow Clock Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core: 400 [MHz]</td>
<td>Core: 400 [MHz]</td>
</tr>
<tr>
<td>PCI: 33 [MHz]</td>
<td>PCI: 33 [MHz]</td>
</tr>
<tr>
<td>DDR: 100 [MHz]</td>
<td>DDR: 100 [MHz]</td>
</tr>
<tr>
<td>SDR: 66 [MHz]</td>
<td>SDR: 66 [MHz]</td>
</tr>
<tr>
<td>Commit: 0</td>
<td>Commit: 0</td>
</tr>
</tbody>
</table>

Enable

PSR Data

 PLL Counter

Wake event

Control Logic

Global Clock Enable
## Programming Interface
### Processor and Northbridge

#### Adaptive Power Control
**CPU interface**

<table>
<thead>
<tr>
<th>CPUID 8086 0001h</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>EDX:0</td>
<td>LongRun supported</td>
</tr>
<tr>
<td>ECX</td>
<td>Nominal core frequency</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPUID 8086 0007h</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>EAX</td>
<td>Current core frequency</td>
</tr>
<tr>
<td>EBX</td>
<td>Current core voltage</td>
</tr>
<tr>
<td>ECX</td>
<td>Current performance percentage</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MSR 8086 8010h</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>EDX</td>
<td>Upper boundary (% of max. performance)</td>
</tr>
<tr>
<td>EAX</td>
<td>Lower boundary (% of max. performance)</td>
</tr>
</tbody>
</table>

#### Advanced Thermal Control
**Northbridge interface**

<table>
<thead>
<tr>
<th>Function 0, Register A8h</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 4</td>
<td>Thermal Management enabled</td>
</tr>
<tr>
<td>Bit 1:3</td>
<td>Power reduction level</td>
</tr>
<tr>
<td>Bits</td>
<td>Mode</td>
</tr>
<tr>
<td>000</td>
<td>Reserved</td>
</tr>
<tr>
<td>001</td>
<td>Reserved</td>
</tr>
<tr>
<td>010</td>
<td>75.0%</td>
</tr>
<tr>
<td>011</td>
<td>62.5%</td>
</tr>
<tr>
<td>100</td>
<td>50.0%</td>
</tr>
<tr>
<td>101</td>
<td>37.5%</td>
</tr>
<tr>
<td>110</td>
<td>25.0%</td>
</tr>
<tr>
<td>111</td>
<td>12.5%</td>
</tr>
</tbody>
</table>

| Bit 0                    | LongRun supported                                               |
Energy Efficiency
Superior Performance in Small Form Factors

CPUmark99

Power [W]

All-Day Computing

Crusoe TM5600

Conventional Mobile x86

Battery

Active (fan)

Passive

Cooling Barrier

A/C

Superior Performance in Small Form Factors

16th Hot Chips Symposium - August 15, 2000
The LongRun Advantage
DVD Playback - Performance on Demand
### Power Comparison

**Substantial Power Reduction, Delivered by Crusoe**

#### Conventional Mobile x86 Solution

<table>
<thead>
<tr>
<th>Mode</th>
<th>Processor</th>
<th>North Bridge</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal (C0)</td>
<td>650 / 500 MHz</td>
<td>3.3 V</td>
<td>650 / 500 MHz</td>
</tr>
<tr>
<td></td>
<td>1.6 / 1.35 V</td>
<td></td>
<td>1.6 / 1.35 V</td>
</tr>
<tr>
<td>AutoHALT (C1)</td>
<td>1.7 / 1.1</td>
<td>2.0</td>
<td>3.7 / 3.1</td>
</tr>
<tr>
<td>Quick Start (C2)</td>
<td>1.3 / 0.8</td>
<td>2.0</td>
<td>3.3 / 2.8</td>
</tr>
<tr>
<td>Deep Sleep (C3)</td>
<td>0.5 / 0.3</td>
<td>~1.0</td>
<td>1.5 / 1.3</td>
</tr>
</tbody>
</table>

#### Crusoe TM5400 Integrated North Bridge

<table>
<thead>
<tr>
<th>Mode</th>
<th>LongRun</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>633 / 300 MHz</td>
</tr>
<tr>
<td></td>
<td>1.6 / 1.2 V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Watts</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.5</td>
</tr>
<tr>
<td>0.9</td>
</tr>
<tr>
<td>0.6</td>
</tr>
<tr>
<td>0.05</td>
</tr>
</tbody>
</table>

Crusoe plays Soft-DVD at the same power that conventional mobile x86 processors use in Deep Sleep!
The LongRun Advantage
DVD Playback - Thermal Comparison

Conventional Mobile x86 Processor

- **105.5° C**
- **221.9° F**
- Active thermal solution required
  (Fan or overload protection)

Crusoe TM5400 Processor with LongRun

- **48.2° C**
- **118.8° F**
- Passive thermal solution
  (No fan or overload protection)
Summary

- **Crusoe Supports the x86 Power Management Model with Significantly Reduced Power Consumption**
  - Sleep: $4 \times (C1) - 30 \times (C3)$ power savings

- **Crusoe Leverages Code Morphing Software to Drive Performance on Demand - LongRun**
  - Normal: $2 \times - 10 \times$ power savings

- **Crusoe Leverages LongRun to Expand the Thermal Budget**

- **Crusoe’s Innovative Low-Power Technology Portfolio**
  - Enables a whole new class of battery-powered devices
  - The full PC and Internet experience - Anywhere and Anytime