The Network Processor Revolution

Fast Pattern Matching and Routing at OC-48

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Market Segments

1. **Optical Core**
   - DWDM Ring
     - OC–192 to OC–768

2. **Carrier Network**
   - Carrier Core
     - OC–48 to OC–192, 10 GbE
   - Carrier Edge
     - OC–48 to OC–192, 10 GbE

3. **Metro Area Network**
   - Metro Core
     - OC–48 to OC–192, 10 GbE
   - Metro Edge
     - OC–48 to OC–192

4. **Access Network**
   - Access Ring
     - OC–3 to OC–48
   - Access Network
     - OC–48 to OC–192

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Agere’s Approach

- Family of Chips for Network Devices
- New “Data-Flow” Approach
- High-level Software Programming

What are the old approaches?
Old Approach

- Worked well for awhile
- Higher speeds, more functionality needed
- Started falling behind dramatically

Diagram:
- Speed
- Time
- Network Bandwidth
- Processor Speed (Moore's Law) 2X per 18 months
Old Approach #2

- Develop custom ASIC to perform wirespeed routing/queuing
  - High development costs
  - Long time to market
  - No flexibility (e.g. IPv6 = forklift upgrades, Diffserv = forklift upgrade)
Agere’s Approach

- Highly pipelined chip-set for fast “Data Path”

Wire-speed Path
- Forwarding
- Shaping
- Queuing
- SAR
- Monitoring, etc.

Data Path

Data in \rightarrow Data out

Slow-speed Path
- Routing protocols
- Error processing
- Statistics reporting
- Configuration, etc.

Control Path

μP
Agere’s Approach

- Agere chip-set forms the wire-speed path

![Diagram showing Agere's chip-set approach](image-url)
System Overview

- Fast Pattern Processor (FPP)
System Overview - FPP

- Recognition/Classification/Filtering
- Functional Processing
- Assembly (if necessary)
System Overview - FPP

**Features**
- Programmable classification up to Layer 7
- Functional Programming Language
- Highly pipelined multi-threaded processing of PDUs
- ATM re-assembly at OC-48c rates
- Table lookup with millions of entries & variable entry lengths
- Configurable UTOPIA/POS interfaces

**Benefits**
- Time to market, ease of upgrade
- Reduces development time, code maintenance
- High performance scalable architecture
- Eliminates external SAR
- Eliminates need for external CAMs; deterministic performance regardless of table size
- Simplifies design and reduces development cost
System Overview - FPP

- Input Framer
- SDRAM Control
- Output Interface
- Block Buffers and Context Memory
- Pattern Processing Engine
- Queue Engine
- Functional Bus Interface
- Configuration Bus Interface
- SSRAM
- 32-bit Utopia/POS from PHY
- 8-bit POS from ASI
- 32-bit POS to RSP
- Functional Bus to ASI
- 8-bit Configuration Bus from ASI

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System Overview

- Routing Switch Processor (RSP)
System Overview - RSP

- Transmit queuing
- Traffic Management and Shaping
  - Quality of Service (QoS), Class of Service (CoS)
- Packet Modification
  - Including Segmentation
System Overview - RSP

**Features**

- **64K queues**
  - programmable shaping (such as VBR, UBR, CBR)
  - programmable discard policies
  - programmable QoS/CoS
  - 16 levels of priority
- **Programmable packet modifications**
- **Support for Multicast**
- **Highly pipelined processing of PDUs**
- **OC-48c bandwidth**
- **Generates required checksums/CRC**

**Benefits**

- **Large number of connections**
  - OEM Differentiation
  - Enables new policy based management system
- **Support for emerging apps**
- **Consistent software model across all programmable features**
- **High performance architecture**
- **Smart processing at very high bandwidths**
System Overview - RSP

Input Interface

Assembly

Stream Editor

Output Interface

SDRAM

SSRAM

Context

Buffer Management

Transmit Request

Flow Control

Queue Manager

Traffic Mgmnt. Engine

Traffic Shaping Engine

Transmit Queue

SSRAM

SSRAM

SSRAM

32-bit POS from FPP

8-bit Configuration Bus from ASI

8-bit POS to ASI

32-bit Utopia/POS to backplane

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Chip Details (Payload Plus Chipset)

- TSMC 0.18um technology
- 26.4 million transistors
- 1.33 million RAM bits
- Measured Power Consumption: 6.2W
Software Landscape

**FPL Code**
(Functional Programming Language; defines classification)

**Control Code**
(interfaces to chipset via Agere RTE and APIs)

**ASL Scripts**
(Agere Scripting Language; defines policing, traffic management, shaping and modification)

Data in

PHY

FPP

RSP

BPI

Data out

μP

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Functional Programming Language (FPL)

- FPL is a high-level language expressly designed for high-speed protocol processing
  - Fast pattern matching of the data stream
  - Easy-to-understand statement semantics
  - Dynamic updating of FPL programs in the FPP
  - A complete software development tool set
### FPL IP Processing Example

```
IP: IPv4_header fskip(36) dest=route fTransmit(dest);
```

<table>
<thead>
<tr>
<th>VER</th>
<th>HL</th>
<th>Service Type</th>
<th>Total Length</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Identification</td>
<td>Flags</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Time to Live</td>
<td>Protocol</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Source Address</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Destination Address</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>IP Options</td>
<td></td>
</tr>
</tbody>
</table>

```
route: 10.20.15.12  freturn(FILTER)
route: 10.20.15.*   freturn(LOCAL)
route: 10.20.*.*    freturn(GATEWAY)
```
Performance: IPv4 4-tuple (ATM)

Payload Plus Chipset operating at 133Mhz
IP over ATM over SONET
Performance: IPv4 4-tuple (POS)

Payload Plus Chipset operating at 150Mhz
IP over PPP over SONET
Payload Plus Chipset operating at 133Mhz
IMIX = 55% 64byte, 5% 72byte, 17% 596byte, 23% 1520byte

Agere Systems, Inc.
Payload Plus Chipset operating at 133Mhz
IMIX = 55% 64byte, 5% 72byte, 17% 596byte, 23% 1520byte
PayloadPlus™ Summary

- **Value Add Elements**
  - Classification
  - Statistics Gathering
  - Buffer Management
  - Traffic Shaping
  - Data Modifications

- **Hardware Overhead**
  - Linked List Maintenance
  - Queue Maintenance
  - Parallel Processing
  - Pipeline Processing

**OC-48c Classification, Scheduling, Statistics**

133MHz, 6.2W
Backup Slides
Building Blocks for Wire-Speed Datapath

Wire-speed Datapath

- **PHY, Framer**
- **FPP - Fast Pattern Processor**
  - Classification engine
- **VPP - Voice Packet Processor**
  - AAL2 Co-processor
- **RSP - Routing Switch Processor**
  - Queuing, QoS, CoS, Modification
- **ASI - Agere System Interface**
  - Policing, Statistics, PCI bridge

Non “Wire Speed” µP

Control Plane: Protocol Stacks, Applications

IP, POS, ATM and Frame Relay at OC-48c Rates

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FPL is to Communication Apps what SQL is to Relational Databases

<table>
<thead>
<tr>
<th>Focus</th>
<th>Communications</th>
<th>Generic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hides parallelism</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Real-time capable</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Good for routing/switching</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Good for spreadsheets</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Wide variety of prog. styles</td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>

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System Overview - Applications

- Building-blocks approach allows flexibility
  - Many different applications possible
  - Mix-and-match chips for desired functionality

GbE/POS Line Cards

OC-48c ATM Line Cards

Router Card

Legacy I-Face

OC-48 SAR

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