VASA: Single-chip MPEG-2 422P@HL CODEC LSI with Multi-chip Configuration for Large Scale Processing beyond HDTV Level


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Nippon Telegraph and Telephone Corporation
Japan
Outline

- History of MPEG-2 Chips in NTT
- Background and Motivation
- Key Features and Functions
- Main Architecture
- Chip Implementation
- Software Architecture
- Multi-chip Applications
- Summary
History of MPEG-2 Chips in NTT

- Enc-C, Enc-M (‘95) 
  (Hot Chips 7)

- Low delay

- Portable HDTV Encoder (ICCE2001)

- High compression

- Multi-chip HDTV

- Encoding PC card (ICCE2000)

- High quality

- SuperENC (‘98)  
  (Hot Chips 10)

- SuperENC-II (‘00)

- Single-chip HDTV

- VASA (‘02)  
  (Hot Chips 14)

- VASA: Versatile Advanced Signal processing Architecture

- Very small HDTV board/module
- Various professional systems
- New applications beyond HDTV level

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Background and Motivation

- Global wave of digitization in TV broadcasting.
  - Terrestrial digital broadcasting will start in Japan in 2003. Producing programs and exchanging them over broadband digital network will boost their circulation.

- Professional and compact HDTV CODEC systems.
  - 1U half-rack -> Very small board/module
  - 9-chip HDTV -> Single-chip HDTV

- Requirements:
  - Small space & low power consumption
  - New applications beyond HDTV level

**VASA: New Single-chip MPEG-2 422P@HL CODEC LSI with Multi-chip Configuration**
Key Features and Functions

- Single-chip Applications:
  - Traditional and advanced high quality CODEC (encoding/decoding),
  - Pre-processing for extracting picture characteristics
  - Watermarking for digital content protection

- Multi-chip Applications:
  - Large scale processing beyond HDTV level for digital cinema and multi-angled live TV
  - Multi-view profile for stereo image CODEC
  - Multi-channel CODEC with TS multiplexing and de-multiplexing
Main Architecture (Approach)

- Re-modeling of “Parallel Encoding”
  - Previous: Individual address spaces model
  - Current: Unique address space model

- Control and data hierarchy
  - Macroblock pipeline schemes in each parallel encoding core (intra-core) and inter-core (intra-chip: top)
  - Two level memory hierarchy for intra- and inter-core

- HFCA: Hierarchical Flexible Comm. Architecture
  - Dual hierarchical backbones linked to every module
    - Small control information: CPU-BUS
    - Huge picture data information: System-BUS
Spatial/temporal flexibility in data transfer via software on **DIF** in each core and on **MIF** in a chip
Main Architecture (Inter-chip Communication)

- Multi-chip configuration (scalability) for large scale processing beyond HDTV level
Main Architecture (Summary)

HFCA (with MIF & DIF) Feature and Functions:

- **Space and time switching:**
  
  Data transfer between each chip, core, module, and sub-module immediately or after a certain time interval in the same manner.

- **Hierarchical structures:**
  - CPU-BUS: TRISC + VRISC x 3
  - System-BUS: MIF + DIF x 3

- **Controlling DDR-SDRAM and optimizing its active bandwidth**
  - Ordinal encoding: 70% (average ratio)
  - Advanced encoding: 85% (average ratio)

- HFCA provides sufficient performance and flexibility for recent high quality CODEC technologies.
Photograph of VASA
# VASA Physical Features

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.13-(\mu\text{m}) 8-level metal CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of transistors</td>
<td>61.4 million</td>
</tr>
<tr>
<td>Die size</td>
<td>14.0 mm x 14.0 mm</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>200-MHz</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>Core: 1.5V / I/O:3.3V / DDR: 2.5V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>3.0 W (at 1080I 422P@HL)</td>
</tr>
<tr>
<td>Package</td>
<td>1008-pin FCBGA (35 mm x 35 mm)</td>
</tr>
<tr>
<td>External memories</td>
<td>256Mbit (32-bit) 200MHz DDR-SDRAM x2 (for images) and 32Mbit (16-bit) 100MHz SDRAM x1 (for TRISC large firmware, <em>if necessary</em>)</td>
</tr>
</tbody>
</table>
## VASA Functional Features

<table>
<thead>
<tr>
<th>Video: Profile and level</th>
<th>MPEG-2 {422P,MP}@HL, {422P,MP}@H-14,{422P,MP,SP}@M</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>narrow: -225.5/+211.5 (H), -113.5/+125.5 (V)</td>
</tr>
<tr>
<td></td>
<td>wide: -449.5/+435.5 (H), -128.0/+127.5 (V)</td>
</tr>
<tr>
<td>Search range</td>
<td>single-chip: 1920/1440 x 1080 at up to 30 frames per second</td>
</tr>
<tr>
<td></td>
<td>1280 x 720 at up to 60 frames per second</td>
</tr>
<tr>
<td>Resolution &amp; rate</td>
<td>multi-chip: Max. 4096 x 2048 up to 60 frames per second</td>
</tr>
<tr>
<td>Pre-processing</td>
<td>Macro block based sophisticated functional filter</td>
</tr>
<tr>
<td>Multi-view profile</td>
<td>Stereo image CODEC</td>
</tr>
<tr>
<td>Watermark</td>
<td>Original watermark insertion/extraction</td>
</tr>
<tr>
<td>Audio: I/O format</td>
<td>Liner PCM or encoded stream (AAC)</td>
</tr>
<tr>
<td>User: I/O format</td>
<td>PES format for timecode and other audio and data</td>
</tr>
<tr>
<td>/stem: I/O format &amp; bitrate</td>
<td>MPEG-2 TS (188/204 bytes)  Max. 300 Mbps</td>
</tr>
<tr>
<td>Multi-channel CODEC</td>
<td>Encoding/decoding by TS multiplexing/de-multiplexing</td>
</tr>
</tbody>
</table>
Evaluation and Validation

- Before fabrication,
  HW/SW were carefully evaluated and validated using VCS and ASIC emulator through small- and/or full-size images.

- After fabrication,
  HW/SW were evaluated and validated using VASA CODEC evaluation boards.

- The first silicon is *successfully* implemented with complete software.
VASA Software Architecture

Function Layer
- Custom Functions
- Custom Function Interface

Basic Function

Hardware Control Layer
- Function Interface
- Chip Layer Controller
- TRISC-VRISC Interface
- E-CORE Layer Controller
- Hardware/Software Interface

Hardware Layer
- VASA Hardware
Multi-chip System Configuration

- Host
- Video Slicer or Multiple HDTV Video In
- Audio In
- User In
- Audio Encoder
- User Encoder
- VASA
  - DDR-SDRAM x 2
- Inter-chip comm. using MDT
- Daisy-chained using TS-MUX
- 422P@HL Encoder
- MPEG-2 Transport Stream

Video In
Audio In
User In

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Multi-chip Applications (1)

Super High Definition Images for Digital Cinema

Parallel encoding / decoding

Inter-chip Communications using MDT

Daisy-chained Outputs using TS-MUX

MPEG-2 Transport Stream
Multi-chip Applications (2)

Parallel encoding / decoding

Inter-chip Communications using MDT

MPEG-2 Transport Stream

Daisy-chained Outputs using TS-MUX

Multiple HDTV images for Multi-view/-angled TV
Summary

- Background and Motivation
- VASA Main Architecture
  - Hierarchical Flexible Comm. Architecture
  - Intra-core/-chip & Inter-chip Comm.
- VASA Implementation
  - Chip Specifications
  - Physical & Functional Features
- VASA Software Architecture
- Multi-chip Applications beyond HDTV Level

VASA is a key LSI for implementing various professional MPEG-2 applications in near future.