HOT CHIPS 15

Final Program

HOT Chips 15

A Symposium on High-Performance Chips – August 17-19, 2003
Memorial Auditorium, Stanford University, Palo Alto, CA

Sunday, August 17, 2003

8:30-12:00 **Morning Tutorial** **Chair:** Tadao Nakamura

Test and Reliability Techniques for Robust System Designs

Subhasish Mitra ***Intel***

High quality and reliability of integrated circuits are keys to the design of robust systems using these parts. Hence, quality and reliability are rapidly becoming "features" just like performance, power-consumption and die size, for both computing and communication applications. Economic analysis shows that it is infeasible to achieve the high levels of quality and reliability expected by customers without designing in these features from very early stages of product development. Techniques for designing quality and reliability features will be described and the associated future challenges will be discussed.

The tutorial will include discussions on the cost of quality, manufacturing defects and test methodologies, design for testability, test pattern generation, built-in-self-test, infant mortality of integrated circuits, impact of noise on test and reliability, soft errors, design techniques for soft error protection, concurrent error detection and self-repairing systems. Examples from actual products will be used to illustrate the applicability of these techniques.

Subhasish Mitra is a Senior Staff Engineer at Intel where he works Design for Testability, Reliability, Manufacturability and Debug. He is also a Consulting Assistant Professor in Stanford University's EE Department. Previously, he was the leader of the DARPA-sponsored ROAR (Reliability Obtained by Adaptive Reconfiguration) project at Stanford, and a consultant for Agilent's System Chip Testing project. His research interests include digital testing, fault-tolerant computing, VLSI design and computer architecture. His recent awards includea Recognition Award at Intel for developing a break-through compaction methodology for test cost reduction, and a Best Panel Award at the VLSI Test Symposium.

12:00-1:30 **Lunch**

1:30-5:00 **Afternoon Tutorial** **Chair:** John Wawrzynek

Past and Future of Cryptographic Engineering

Christof Paar ***Ruhr-Universitaet Bochum***

Security has quickly evolved from a rather obscure niche area to an important aspect of today´s IT applications. The recent trend of pervasive computing will make it necessary to integrate security functionality in an extremely broad spectrum of applications, from traditional computers to household appliances. This application range will force many engineers (without training in cryptography) to think about efficient ways of implementing crypto functions, which are the core tools for providing IT security.

This talk will give an overview of the field of IT security, with a strong focus on cryptographic engineering. After discussing the general objectives of IT security, we will introduce the types of practical crypto schemes , case studies that highlight both symmetric and asymmetric (public-key) algorithms and the challenges of implementing them in hardware and software, the architecture of a high performance public-key engine along with the interaction between implementation and security requirements, and an introduction to side channel attacks (perhaps the most important attacks against crypto schemes in the real world). The presentation will conclude with a discussion of future research challenges.

Christof Paar has the chair for Communication Security (www.crypto.rub.de/index_eng.html) at the Horst Gortz Institute for IT Security at the University of Bochum in Germany. As faculty member at Worcester Polytechnic Institute, he founded the Cryptography and Information Security Labs and is co-founder of the CHES (Cryptographic Hardware and Embedded Systems, www.chesworkshop.org) Workshop series. He has received an NSF CAREER award for research in cryptography and reconfigurable hardware. Christof Paar has been teaching cryptography courses in academia and industry since 1995.

5:00-6:00 **Wine and Cheese Reception**

The HOT Chips 15 symposium is sponsored by the Technical Committee on Microprocessors and Microcomputers of the IEEE Computer Society

IEEE COMPUTER SOCIETY

Monday, August 18, 2003

8:45- 9:00 **Welcome, Opening Remarks**
General Chair: **Siamak Arya**
Program Co-Chairs: **Pradeep Dubey, Mike Flynn**

9:00-10:30 **Session 1: Supercomputing**
Session Chair: **John Sell**

- **Red Storm: A 10,000 node system with reliable, high bandwidth, low latency interconnect** Bob Alverson *Cray*
- **Quadrics QsNet II : A Network for Supercomputing Applications**
  Fabrizio Petrini, David Addison, Jon Beecroft, David Hewson, Moray McLaren *Los Alamos*
- **Sub-lithographic Semiconductor Computing Systems**
  André DeHon *Caltech*

10:30-10:55 **Break**

10:55-11:45 **Keynote:** **Chair: Mike Flynn**
Tadashi Watanabe Vice President, High Performance Computing *NEC*

- **The Whole Earth Simulator: World's Fastest Supercomputer**

11:45-12:45 **Session 2: Embedded**
Session Chair: **Howard Sachs**

- **A Multithreaded RISC/DSP Proc. w/ High Speed Interconnect**
  Erik Norden *Infineon*
- **Intelligent Energy Management: an SoC Design Based on ARM926EJ-S** David Flynn *ARM*

12:45- 2:00 **Lunch**

2:00- 3:30 **Session 3: Application Specific Chips**
Session Chair: **Henry Moreton**

- **RAMP-IV: A Low-Power /High-Performance 2D/3D Graphics Accelerator for Mobile Multimedia Applications**
  Ramchan Woo, Sungdae Choi, Ju-Ho Sohn, Seong-Jun Song, Young-Don Bae, and Hoi-Jun Yo *KAIST*
- **TMS320DM310: A Portable Digital Media Processor**
  Deepu Talla, Russ Austen, Dave Brier, Ching-Yu Hung, Derek Huynh, David Smith, Bruce Xiong, Raj Talluri, and Frank Brill *Texas Instruments*
- **ReX: A dNTSC Receiver System on Chip**
  Slobodan Simovich *Dotcast*

3:30- 4:00 **Break**

4:00- 6:00 **Session 4: Wireless**
Session Chair: **Keith Diefendorff**

- **The Architecture of the Intel® PXA800F Cellular Processor**
  Dilip Krishnaswamy *Intel*
- **BCM2132: GSM/GPRS Handset Baseband w/ Integrated EDGE & Media Functions**
  Nelson Sollenberger, Li Fung Chang, Paul Lu *Broadcom*
- **Broadcom WLAN chipset for 802.11 a/b/g**
  Jason A. Trachewsky, Arya Behzad, Reza Rofougaran *Broadcom*
- **A UMTS Baseband Receiver Chip for Infrastructure Applications**
  Sundararajan Sriram, K. Brown, P. Bertrand, F. Moerman, O. Paviot, C. Sengupta, V. Sundararajan, A. Gatherer *Texas Instruments*

6:00- 7:15 **Dinner**

7:15- 8:45 **Panel:** **Disasters I Have Been Involved With**

Moderator: **Nick Tredennick,** ***Editor, Gilder Technology Report***
Panelists: **Bob Cousins,** ***CTO, Storfinity***
Dave Wyland, ***The Wyland Group, Inc.***
Jack D. Grimes, ***Consultant***
Jim Turley, ***Editor, Silicon-Insider***

Tuesday, August 19, 2003

9:00-10:30 **Session 5: Switching and Routing**
Session Chair: **Marc Tremblay**

- **A Single Chip Shared Mem Switch w/ Twelve 10Gb Ethernet Ports**
  Takeshi Shimizu, Yukihiro Nakagawa, Sridhar Pathi, Yasushi Umezawa, Takashi Miyoshi, Takeshi Horie, Akira Hattori *Fujitsu*
- **Terabit Crossbar Switch Core for Multi-Clock-Domain SoCs**
  Uri Cummings *Fulcrum*
- **Adaptive Packet Processor**
  Bill Lynch *Procket*

10:30-11:00 **Break**

11:00-12:30 **Session 6: Security**
Session Chair: **Pradeep Dubey**

- **Multi-Gigabit SSL & TLS Record Layer Protocol Processor and Multi-Gigabit IPSec Processor**
  David Chin, Terry Tham *Broadcom*
- **Continuum Security Processor: Micro-Architecture Overview**
  Srinivas Mantripragada *NetContinuum*
- **Nitrox-II™ Inline Security Processor**
  M. Raghib Hussain *Cavium*

12:30- 1:45 **Lunch**

1:45- 2:35 **Keynote:** **Chair: Alan Smith**
Robert F. Leheny **Director - Microsystems Technology Office** *DARPA*

- **Perspectives on the Future of Microelectronics for Military Systems**

2:35- 2:45 **Short Break**

2:45- 4:15 **Session 7: Potpourri**
Session Chair: **Forest Baskett**

- **Ubicom MASI - Wireless Network Processor**
  David Fotland *Ubicom*
- **A 10 Gbps Ethernet TCP/IP Processor**
  Jianping Xu, Nitin Borkar, Vasantha Erraguntla, Yatin Hoskote, Tanay Karnik, Sriram Vangal, Justin Rattner *Intel*
- **Janus: A Gigaflop VLIW+RISC SoC Tile**
  Pier Stanislao Paolucci *Atmel*

4:15- 4:30 **Break**

4:30- 6:30 **Session 8: Processors**
Session Chair: **John Crawford**

- **An Embedded 600Mhz Synthesized Processor**
  Howard Sachs *Telairity*
- **POWER5: IBM's Next Generation POWER Microprocessor**
  Ron Kalla *IBM*
- **Ultrasparc Gemini: Dual CPU Processor**
  Sanjiv Kapil *Sun*
- **Two New 130nm Itanium 2 Processors for 2003**
  Harry Muljono, Stefan Rusu *Intel*

6:30- 6:45 **Closing Remarks**

Visit our Web Pages for Registration and Conference Details

http://www.hot.org **http://www.hotchips.org**