
HOT Chips 2003

Intelligent Energy Management:

An SoC design based on ARM926EJ-S



THE ARCHITECTURE FOR THE DIGITAL WORLD™



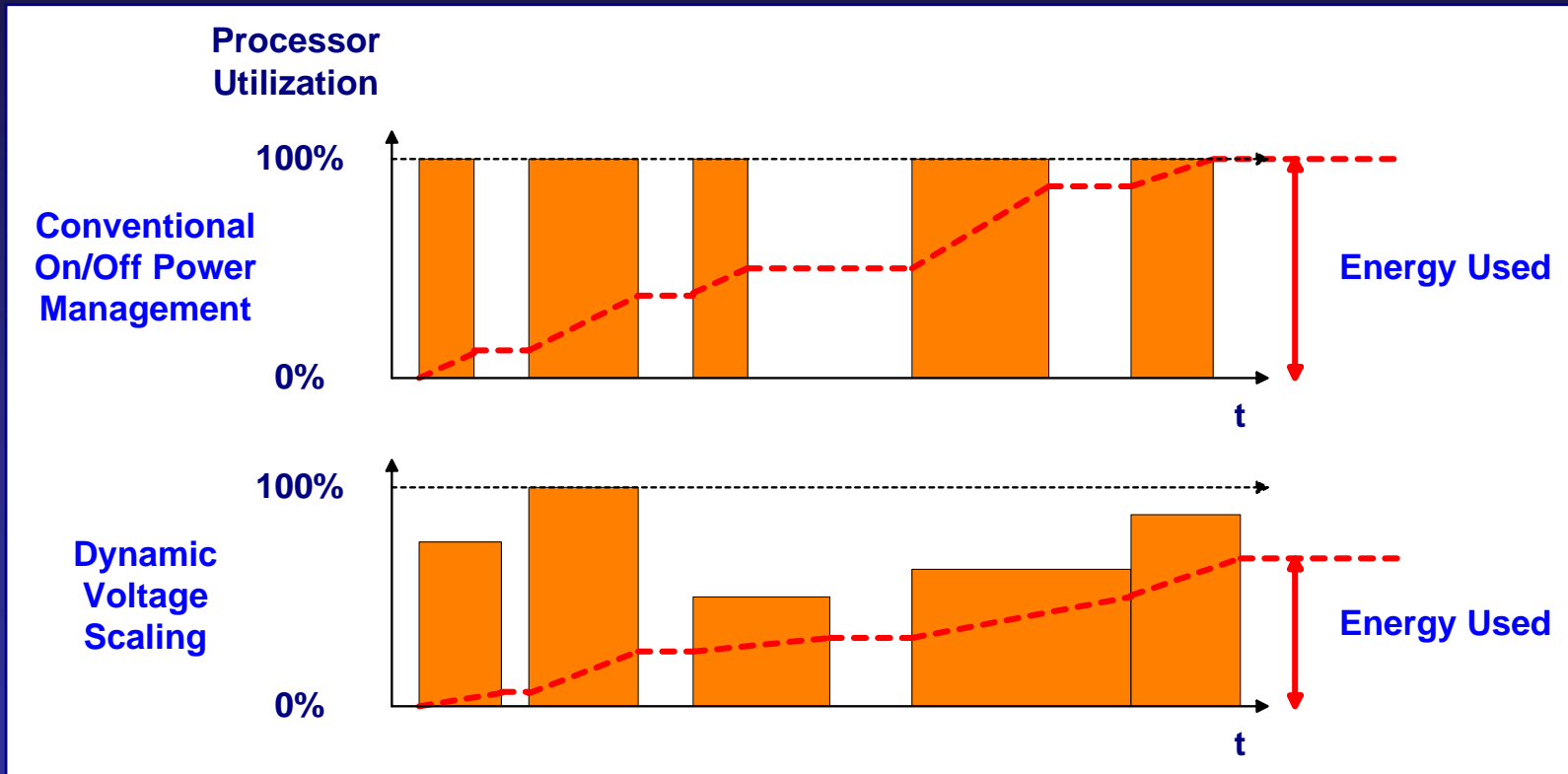
Need for Energy Management

- Today's mobile consumers want:
 - longer battery life *and*
 - smaller, lighter products
- Manufacturers are adding new features and applications to add product appeal:
 - media players (audio, video)
 - gaming
 - video capture
- Increasing processing power requirements and longer battery life are conflicting requirements
- Battery technology alone offers only incremental improvement over the next several years



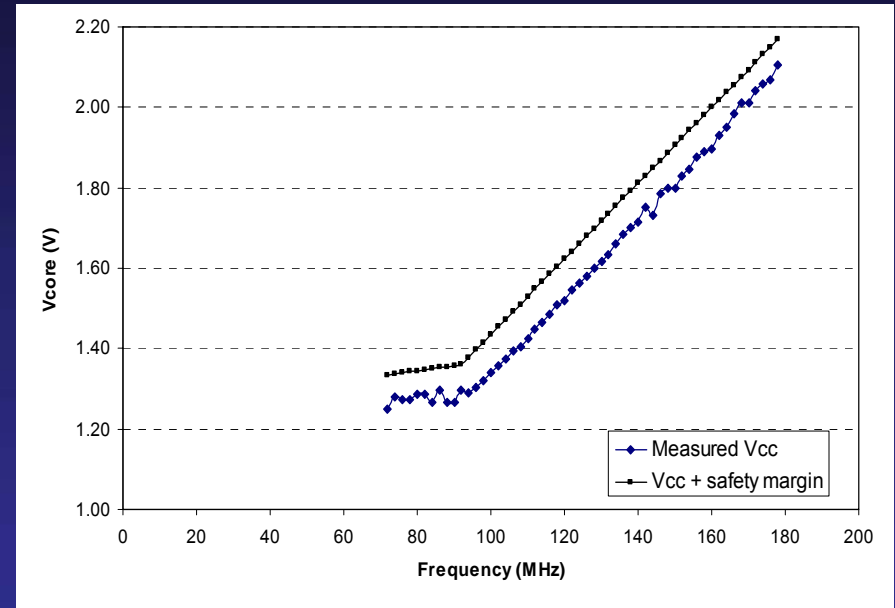
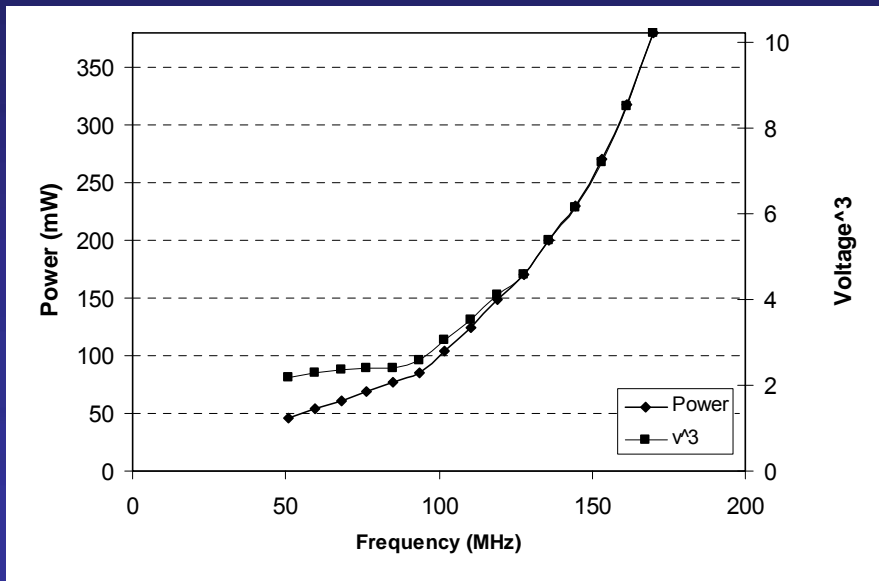
Intelligent Energy Management (IEM)

- Conserving power whilst running = **saving energy**
- Running only fast enough to do the work just in time
- Adapting to changing software workloads



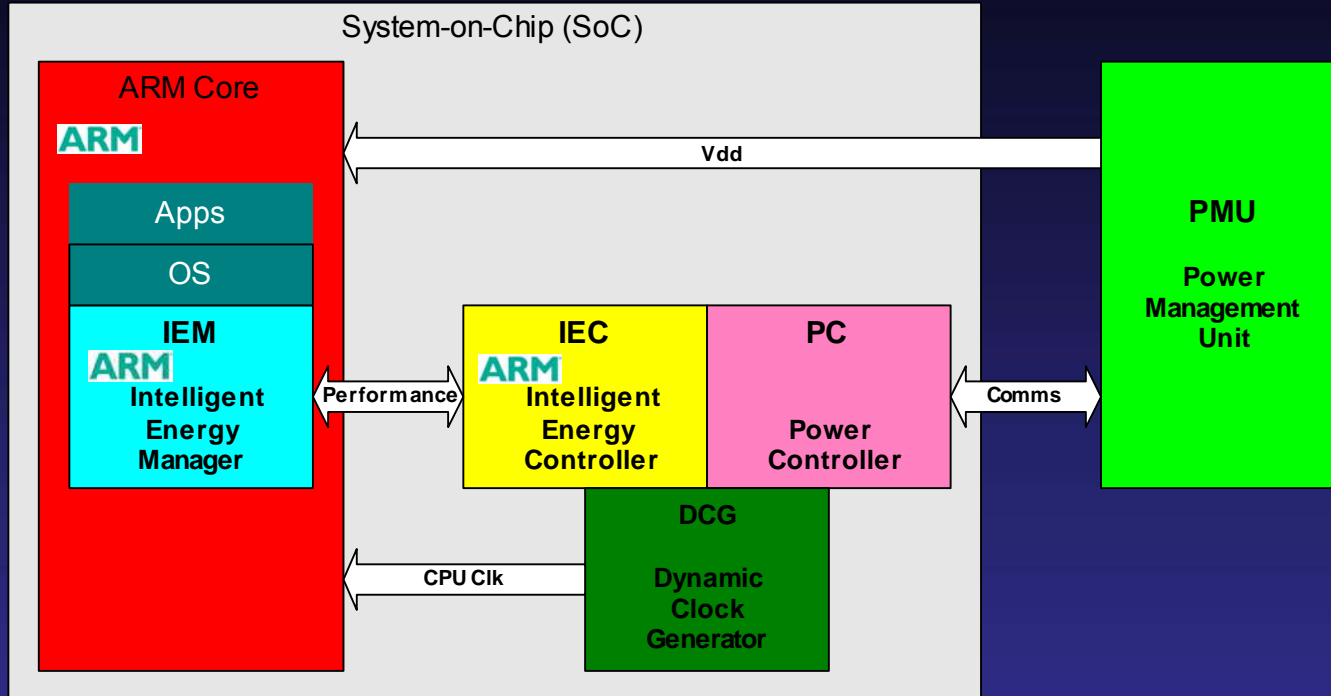
Dynamic Voltage Scaling (DVS)

- Voltage is the only parameter that affects all types of power consumption:
 - Dynamic
 - Static leakage
 - Gate oxide leakage



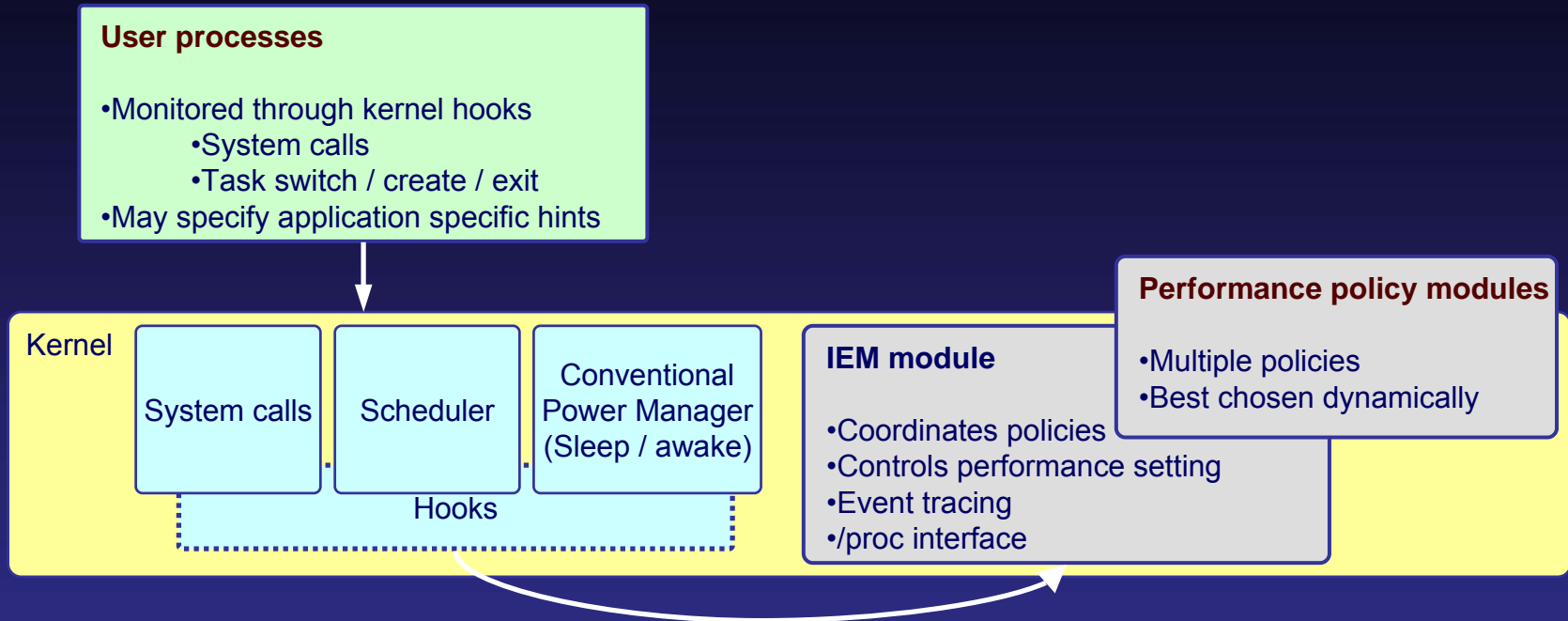
- Intelligent control of DVS designs will bring energy savings

Energy Management System



- IEM and IEC components work together to **predict** lowest acceptable processor performance level
- Power Controller, PMU and Clock Generator work together to **deliver** that lowest performance level

IEM: prediction software



- IEM software uses custom hooks in OS kernel to instrument application software activity
- Multiple algorithms determine performance level requirement for different classes of activity
- **Best global performance determined dynamically**

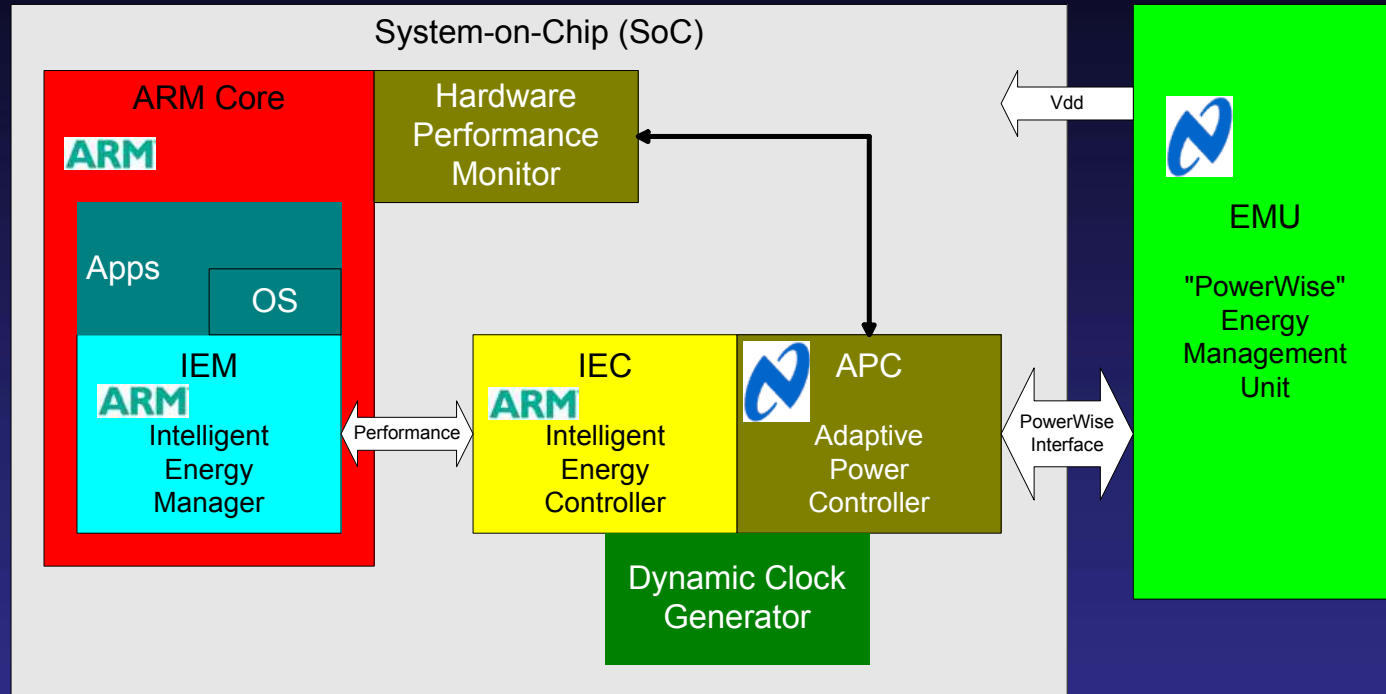
IEC: control and monitoring hardware

- Delivers an abstracted view of the power control and delivery components of the device
- Supplies a 0-100% performance level request to the
 - Power Controller and
 - Dynamic Clock Generator
- Plugs into SoC design as a using a standard ARM AMBA compliant interface (APB)
- Provides hardware assist to IEM software
 - Dynamic performance counters
 - Reduces the monitoring software overhead

Adaptive Voltage Scaling (AVS)

- AVS is a closed loop control mechanism
 - Feedback from the PMU indicates the earliest opportunity to change processor frequency based on the voltage levels being output to the SoC
 - APC monitors the difference between the requested performance level and the actual level achieved
- Taking into account variations due to differences in process technology and ambient temperature the system dynamically changes the voltage applied
- The lowest energy consumption is achieved **OR**
- A specified performance level can be met

AVS Energy Management System

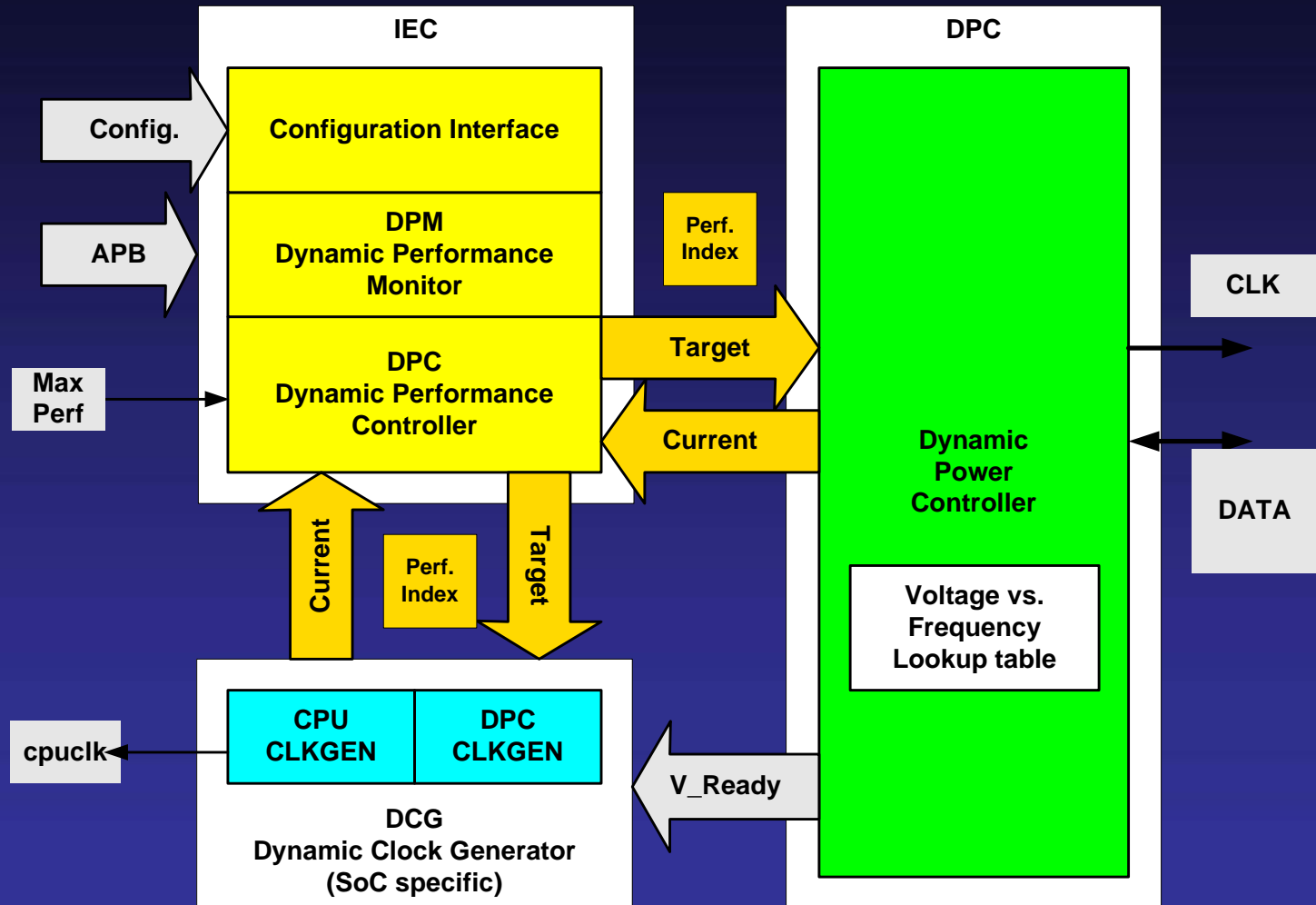


- APC operates in closed loop control mode using HPM to adapt to actual process and temperature
- PowerWise™ Interface provides fast control of EMU and feedback of status for optimum control

PowerWise™ technology

- Adaptive Power Controller (APC)
 - Manages performance level requests
 - Uses hardware monitor to reduce safety margins
- PowerWise Interface (PWI)
 - High-speed, low-power 2-wire comms. interface between APC and SoC-wide power supplies
 - To be published as open standard (9/03)
- Power Management Unit (PMU)
 - High-performance, off-chip power supply
 - Interfaces using PWI
 - Supports open and closed loop control

DVS Control Sub-system



Integration challenges

- Multiple voltage domains (and interfaces)
 - Commercial voltage scaling exploited at chip not SOC level
 - Level-shifter technology abstraction required
 - Builds on power-down and state-retention 'islands'
- Multiple (asynchronous) clock domains
 - Real-time domains typically require fixed clocks
 - Variable voltage domains quantize frequency
 - External memory clock rates often fixed
- External power-control interface handshakes
 - Efficient management of voltage/frequency (PLL) settling times
- Design verification and test
 - Gap between RTL (ideal clocks, implicit power) and layout
 - Static timing analysis and clock distribution in particular

Collaborative SoC Design

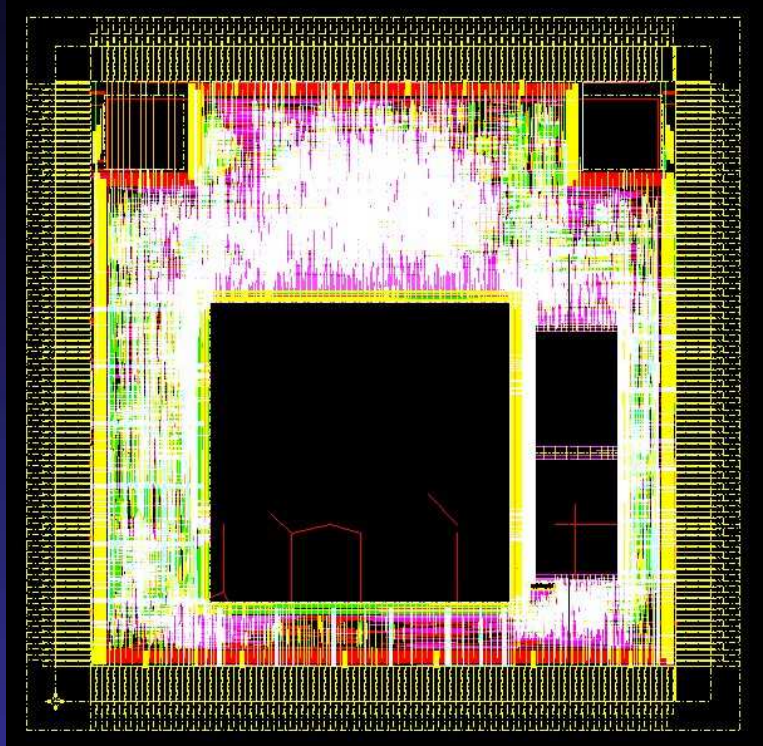
Complete Energy Management solution requires:

- (Off-chip) Power switcher technology
 - Responsive and controllable
- Semiconductor cell/RAM library technology
 - Characterization across voltage/process
 - Level-shifter technology
- On-chip power control technology
- System level design methodology/EDA tools
- Software/API support for OS
 - Predictive performance setting algorithms

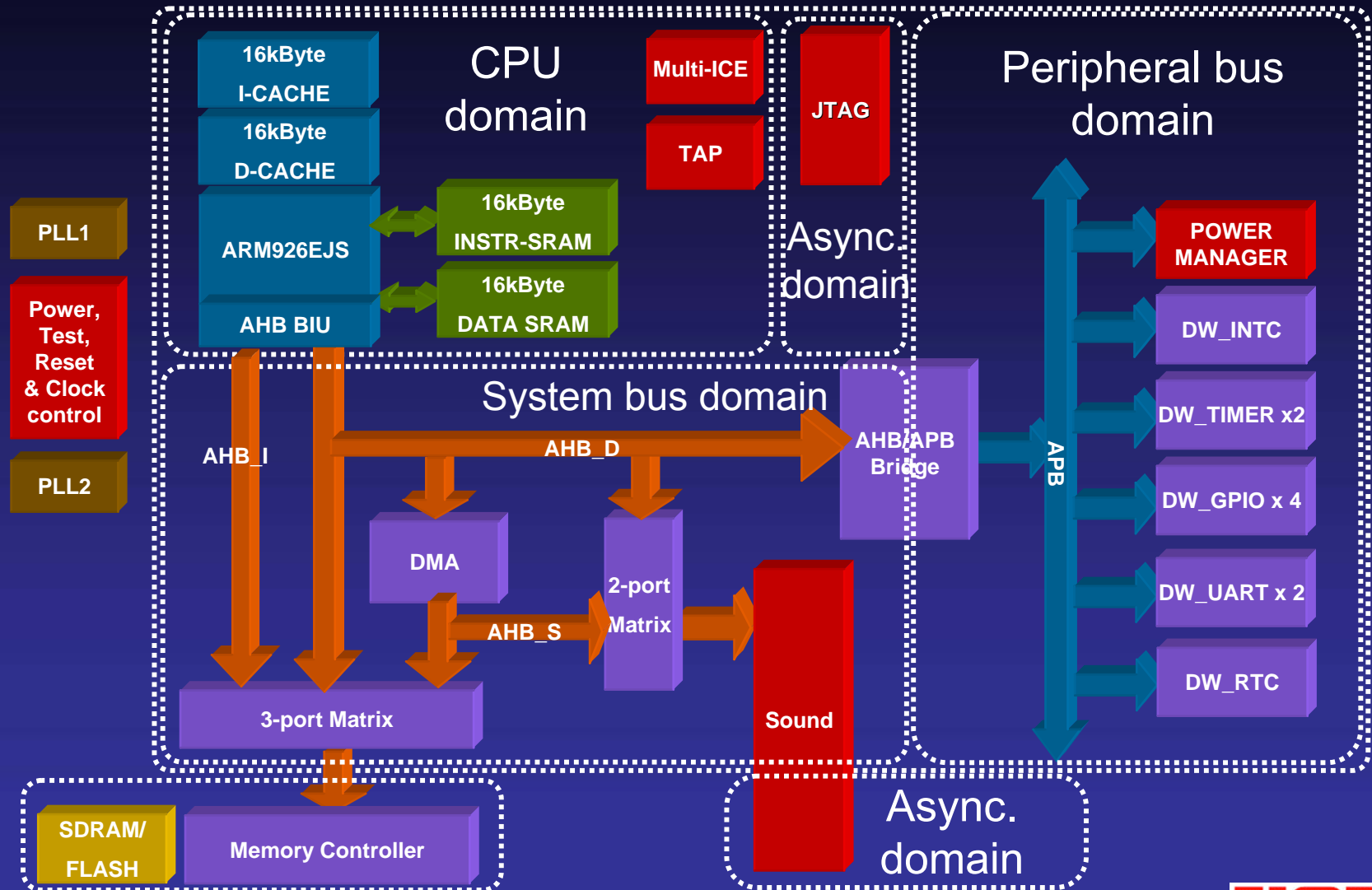
➤ Partnership approach to implementation



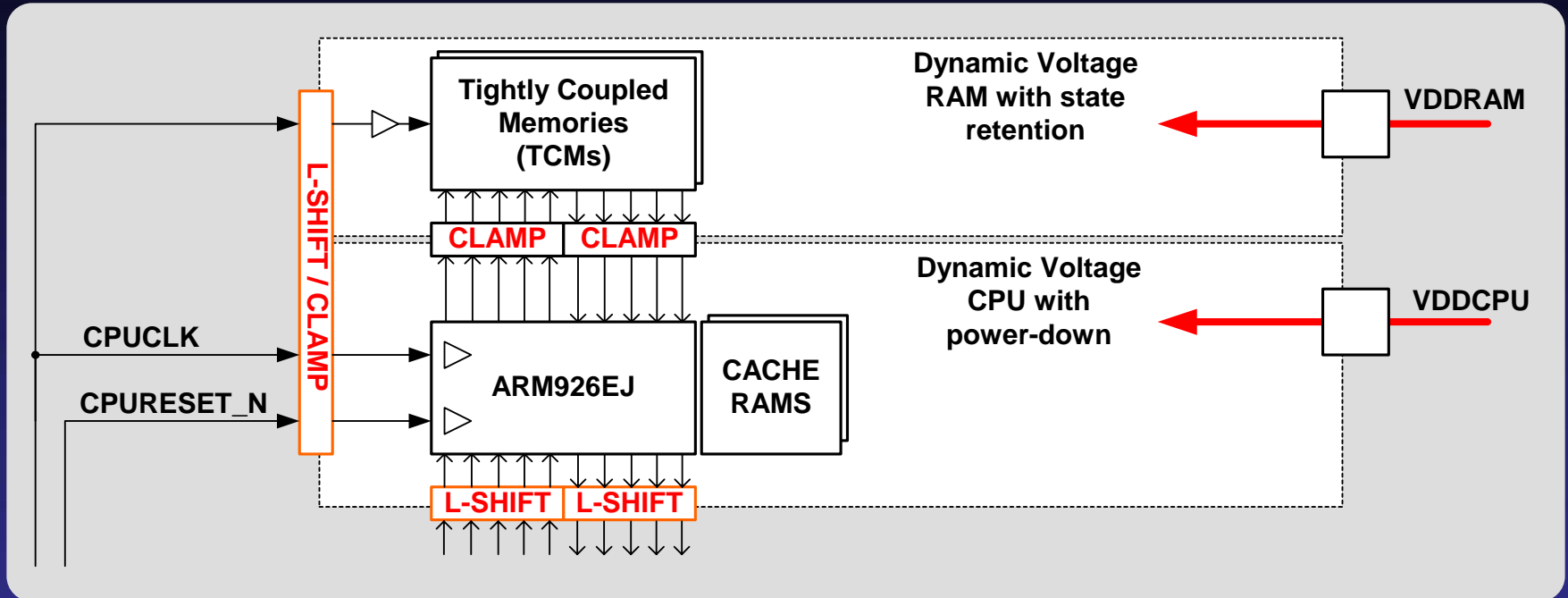
Prototype IEM test chip

- ARM926EJ-S core
 - Multiple power domains
 - Voltage and frequency scaling of CPU, caches and TCMs
 - First full DVS silicon with National Semiconductor PowerWise™ technology
 - NSC Adaptive Power Controller (APC) implemented in FPGA
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- Delivered from TSMC 0.13μm fab. in July 2003
 - Developed by ARM and National Semiconductor using Synopsis EDA tools

IEM test chip power domains

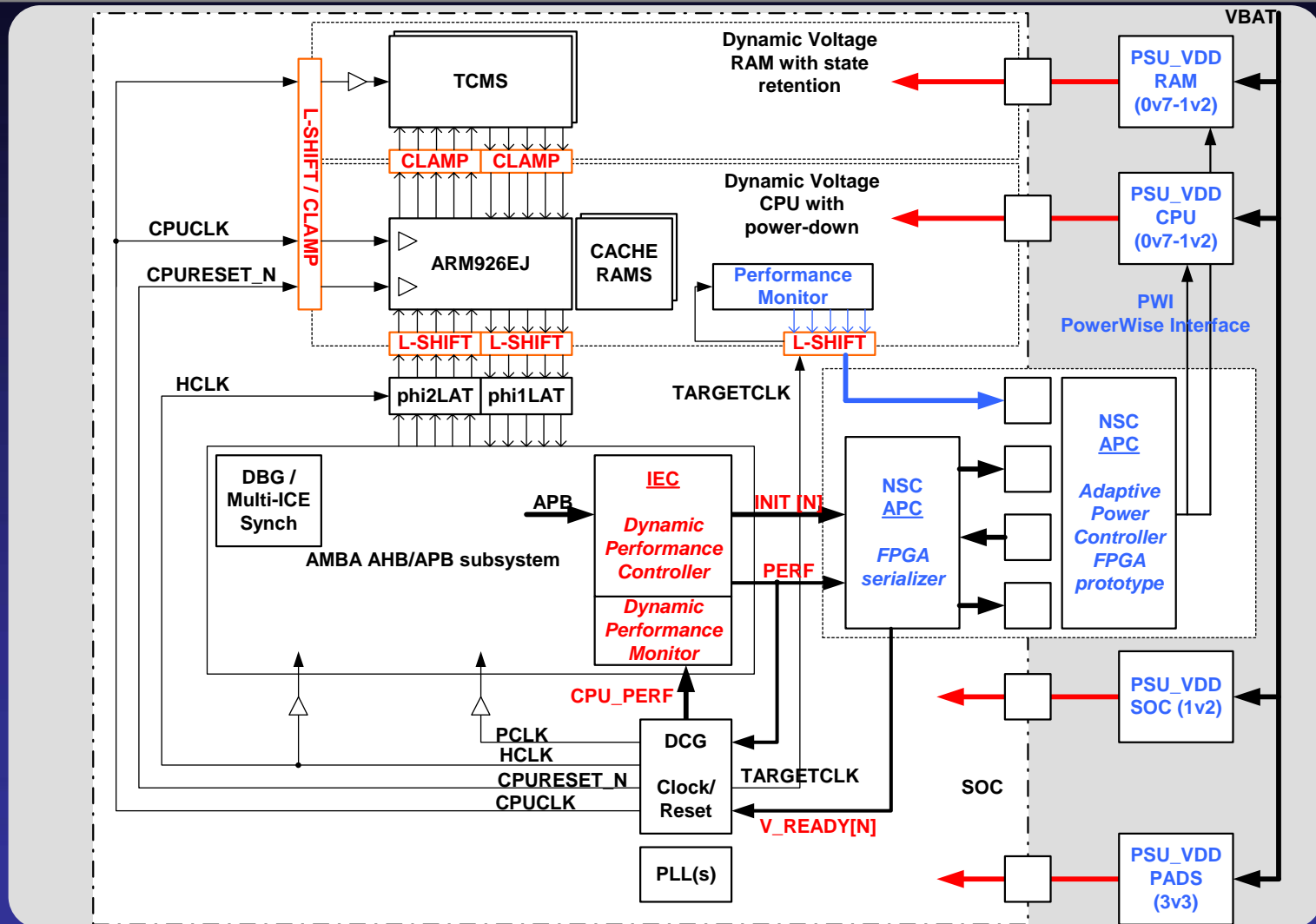


Test chip : CPU subsystem



- Dynamically scale voltage to both CPU and RAMs
 - But support state save to RAM and power-down of CPU
- Level-shifter cells interface to always-powered SOC logic
 - Clamps hold signals low when domain voltage “unsafe”

Testchip : board-level testbench



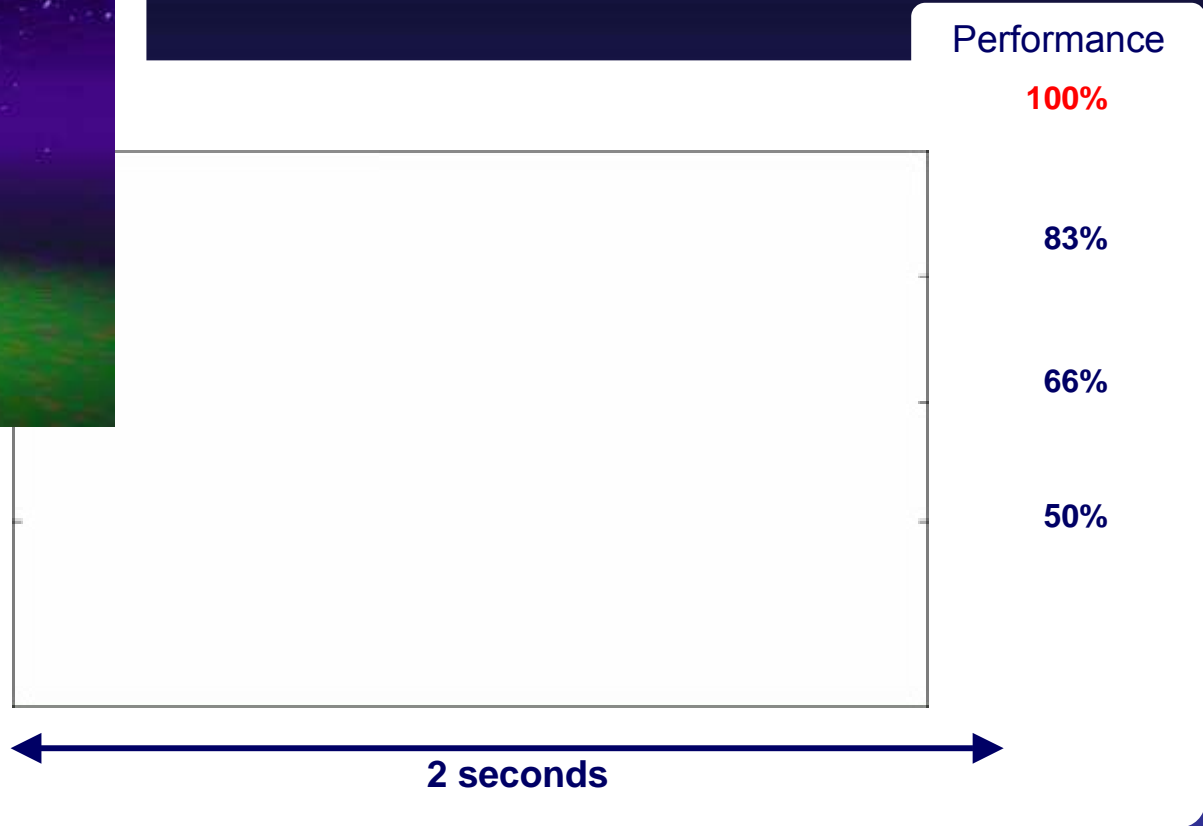
Benchmarking

- Clear requirement to develop benchmarks
 - Standby time taken care of by conventional power management schemes (run/idle/sleep)
 - Focusing on applications processors and smartphone functionality (more “running” time)
 - MP3 players – sound recording
 - MPEG4 video clip players/capture
 - Games – graphics accelerators
 - E-mail and web access (WAP), messaging
 - Need to measure energy saving and quality
- No established benchmarking standards exist today that show quality at low performance

Energy Management in Action



Playing



Wrap Up

- Dynamic performance control is an attractive way of achieving energy management in battery–powered embedded devices **BUT**
 1. There are many challenges at the SoC design level in implementing multiple power domains:
 - Interfacing between power domains
 - EDA tools support
 2. Maximising the benefits of techniques like Dynamic Voltage Scaling requires:
 - SoC designs that include appropriate controls
 - Advanced software to manage performance
 - Standard s/w and h/w interfaces to allow reuse

Intelligent Energy Management

Thank you for listening.

Any Questions?

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