ReX: A dNTSC™ Receiver System-on-Chip

Slobodan Simovich, Ivan P. Radivojevic, T. J. Endres, Tom Bentson, Ray Bingham, Tony Blair, Tom Cowling, Mark Eylander, Rory Fagan, Chris Long, Jim Longino, Dan Olson, Rollen Subia, Doug Whitcomb

Dotcast, Inc.

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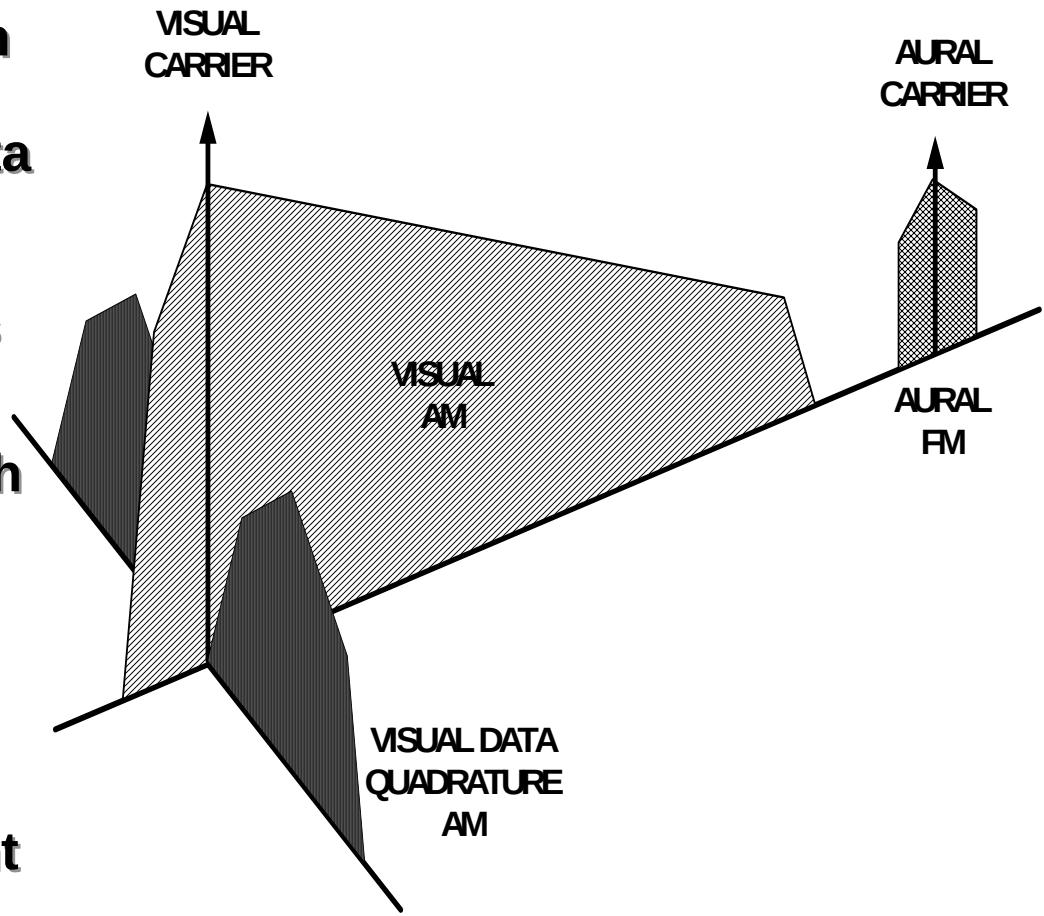
dNTSC™ - General Overview

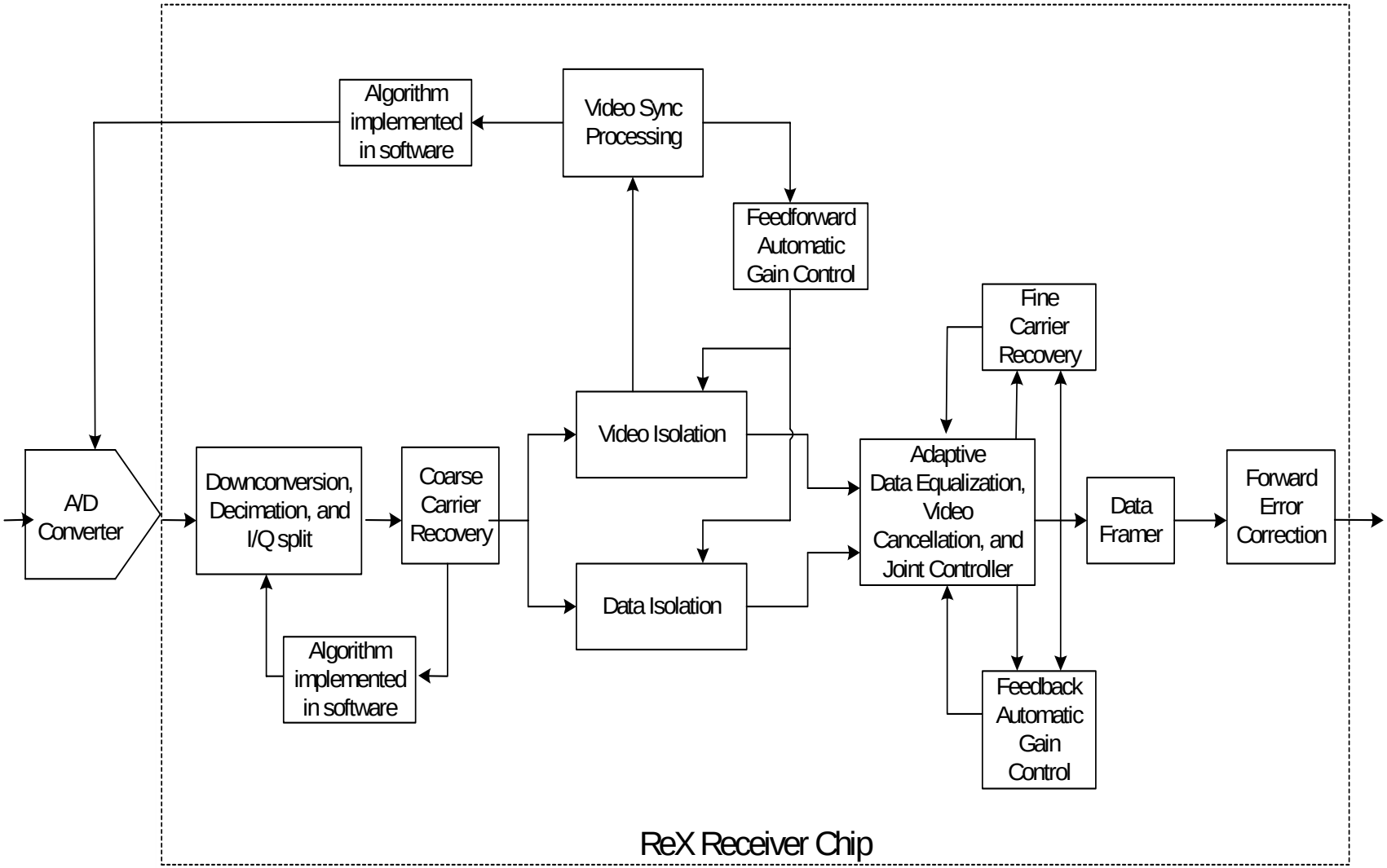
- Datacasting – transfer of data over television
- dNTSC™ – technology for datacasting over analog NTSC television:
  - Up to 4.5Mbit/sec per analog TV channel
  - Receivable within TV station's A-contour at 10^{-8} bit error rate (example: A-contour in Los Angeles - 1.67 million households)
- Obtained FCC license for the deployment of dNTSC™ in June 2002
- Technology developed and productized: modulator, receiver, antenna (for indoor reception)
- Commercial service based on dNTSC™ technology – the MovieBeam™ Service by Walt Disney Corp., scheduled for deployment later this year

dNTSC™ - General Overview

- Visual data is modulated in quadrature with NTSC visual carrier and aural data is negative amplitude modulated on aural carrier - first implementation uses visual carrier, only
- Data inserted coherent with NTSC framing – symbol rate ~613KHz
- Data spectrum is pre-filtered and subcarrier carefully spaced to minimize visual impairment with NTSC television



Receiver DSP Architecture



ReX DSP Architecture

DSP Architectural Features:

- **Visual subcarrier only, 1-3 Mbps, using 4,16,32, 64, or 128 QAM on single subcarrier that is about –26 dB below video (relative to peak of video)**
- **Data spectrum occupies about 1/6 of TV channel, without perceptibly corrupting TV broadcast**
- **Timing recovery, automatic gain control, and data framing derived from visual TV signal**
- **Patent pending adaptive equalization and video cancellation techniques for robust (re)-acquisition in harsh indoor environment**
- **Self-optimizing joint controller (patent pending) for optimum system-level performance is highly programmable with performance-driving features**
- **Field-proven error correction using concatenated Trellis Coded Modulation and a Reed-Solomon block code**

ReX ASIC Architecture

Design Requirements:

- ***Functional robustness*** **– must handle a wide variety of known and less-known phenomena in the field**
- ***High computational performance*** **– the dNTSC decoding algorithm alone requires >15 billion operations/sec (BOPS)**
- ***Low cost*** **– targeted to fit within a budget of a consumer electronics product.**

ReX ASIC Architecture

ASIC Design Philosophy:

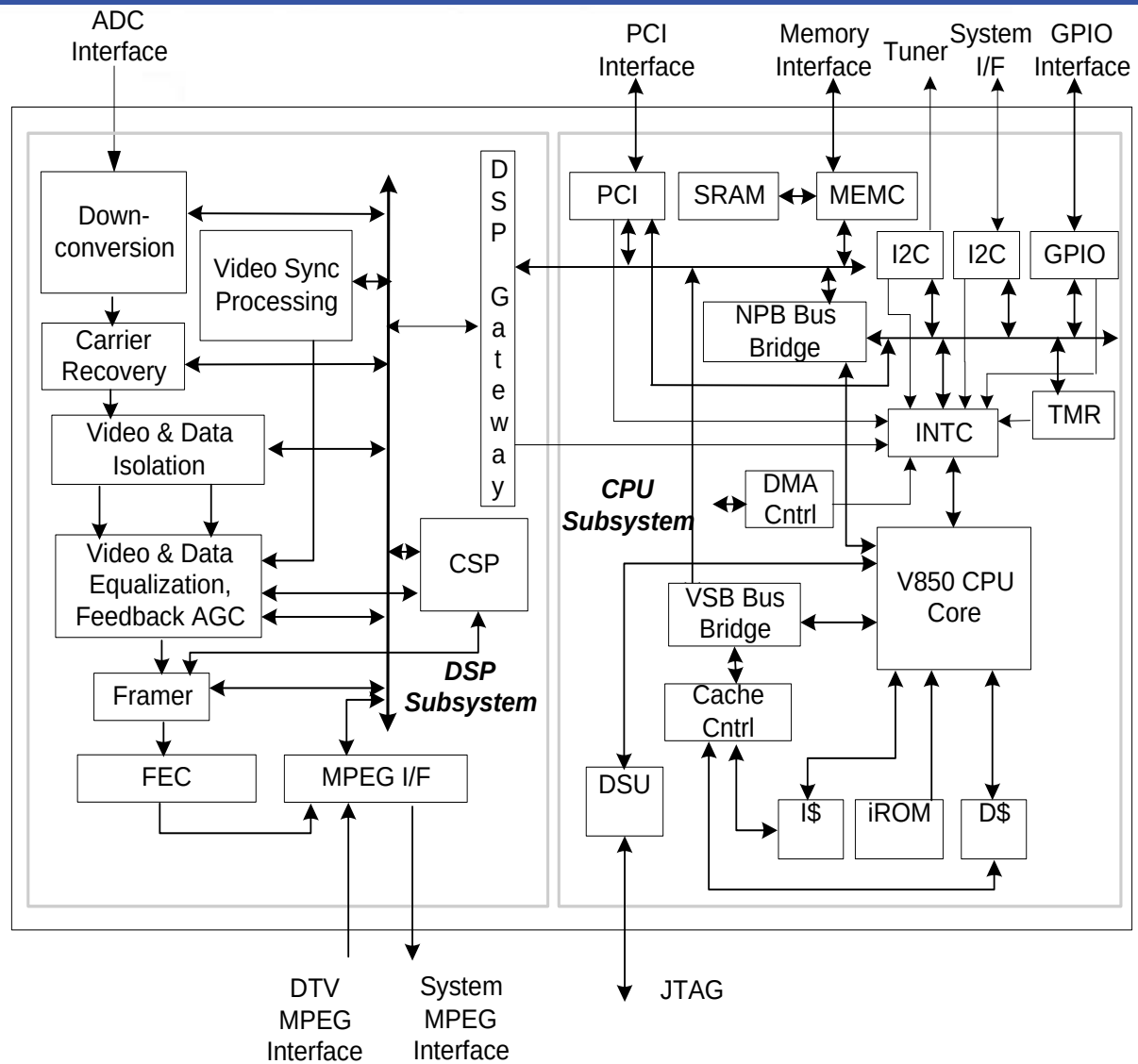
- **Simplicity**
- **Configurability and Programmability**
- **Low-risk fabrication technology**

Implementation Goal: design a robust and reliable mass production part (on a tight schedule, of course)

ReX ASIC Microarchitecture

System-on-Chip:

- **CPU Subsystem – system administrative functions: system I/O, system interrupts, selected DSP applications**
- **DSP Subsystem – dNTSC™ decoding algorithm, FEC, general signal processing**



ReX ASIC Microarchitecture

CPU Subsystem:

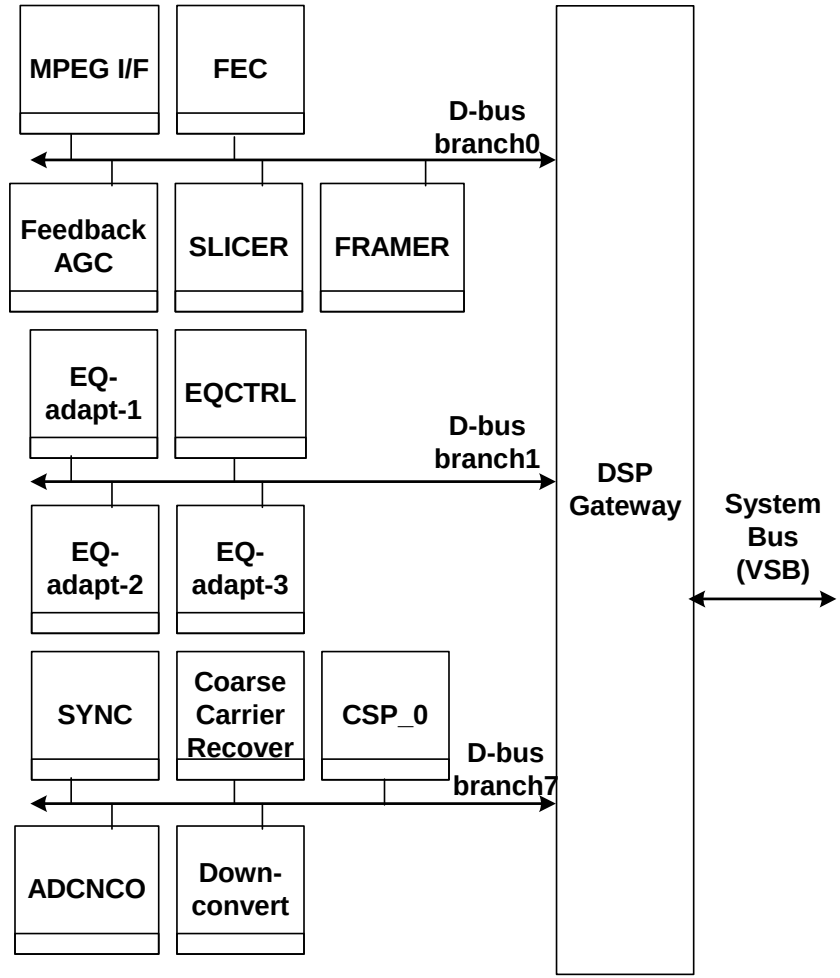
Silicon Technology – NEC's CB-10 (0.25 micron, 5 metal layer)	
CPU core	NU85E (NEC)
System Interface	PCI, I2C, GPIO, MPEG Serial
Tuner Interface	I2C
Clock speed	160/80 MHz
On-chip SRAM	128 KByte
On-chip ROM	16 KByte
Instruction/Data Cache	8/4 KByte
Debug Support	N-Wire/JTAG
External Memory Support	ROM, FLASH, SRAM
OS	ThreadX

Note: CPU Subsystem is ~1/3 of the die area

ReX ASIC Microarchitecture

DSP Subsystem:

- Bus-based system - D-bus
- D-bus agents:
  - Dedicated programmable - FIRs, mixers, FEC, etc.
  - Fully programmable –CSP
- Connectivity: D-bus, and dedicated connections



Note: DSP Subsystem is ~2/3 of the die area

CSP Architecture

Configurable Stream Processor – CSP:

Proprietary general-purpose DSP core (patent pending) optimized for processing of data streams

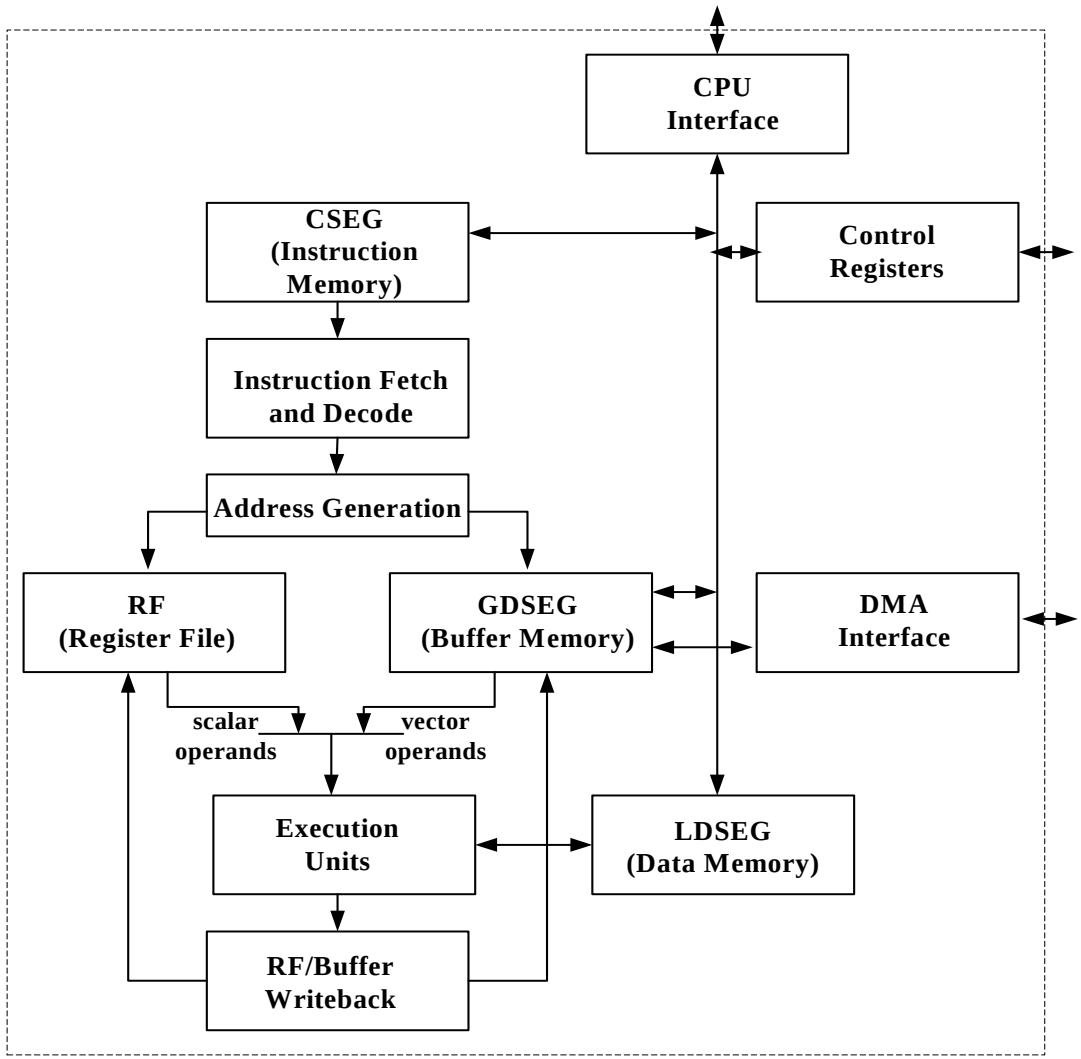
- ISA consists of scalar and vector instructions - implies scalar and vector registers
- Configurable and programmable hardware buffers
- Input/output data stream transfer in parallel with pipe accesses
- Explicit and implicit buffer synchronization mechanisms

CSP Architecture

CSP Pipe:

52 instructions (scalar, vector, bit-wise, push/pop, etc.)

- 8-stage pipe
- 3 memory segments:
  - CSEG (code)
  - GDSEG (buffers)
  - LDSEG (data)
- Configurable buffers - number and size
- Interrupt support

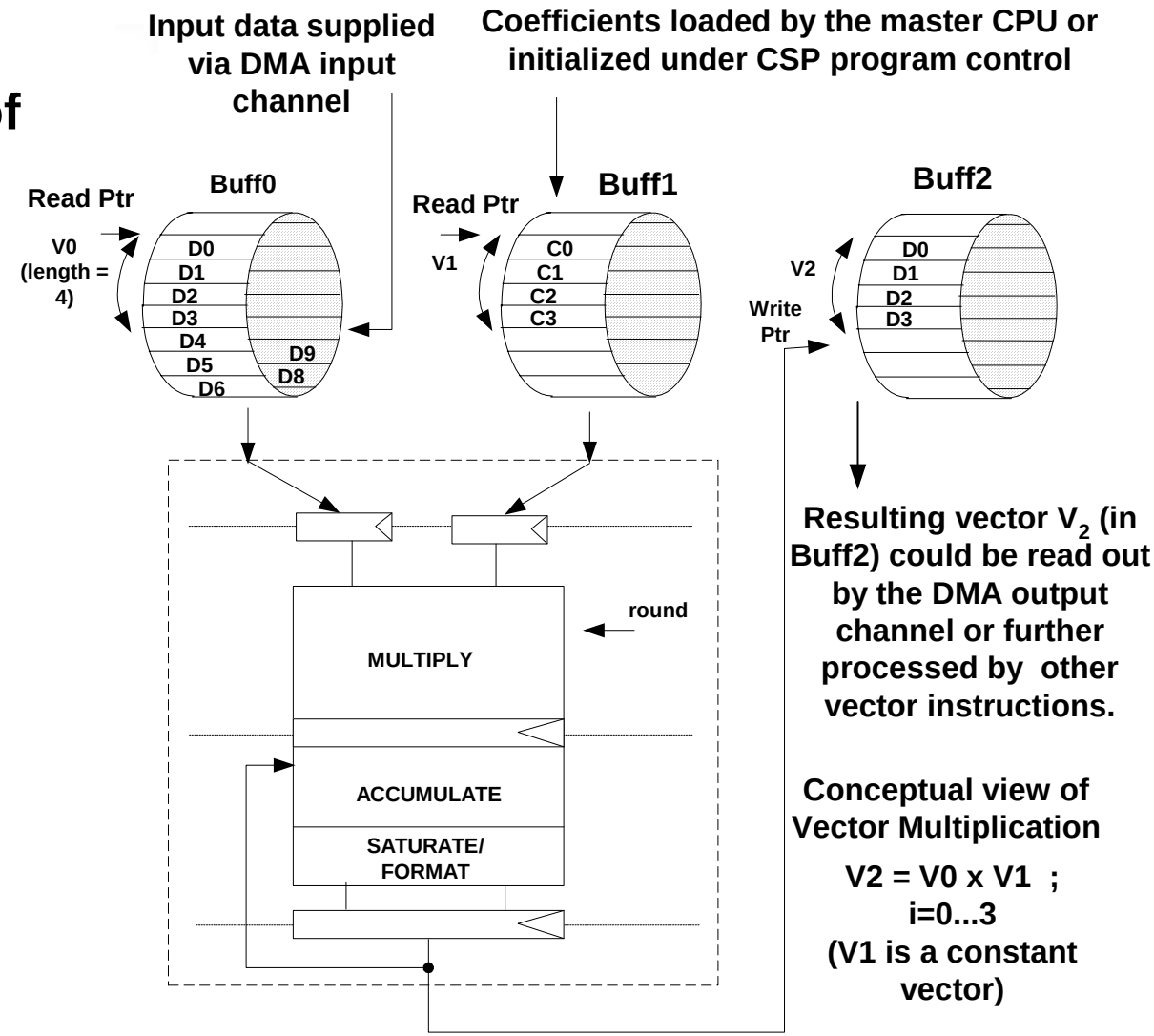


CSP Architecture

Programmable Buffers:

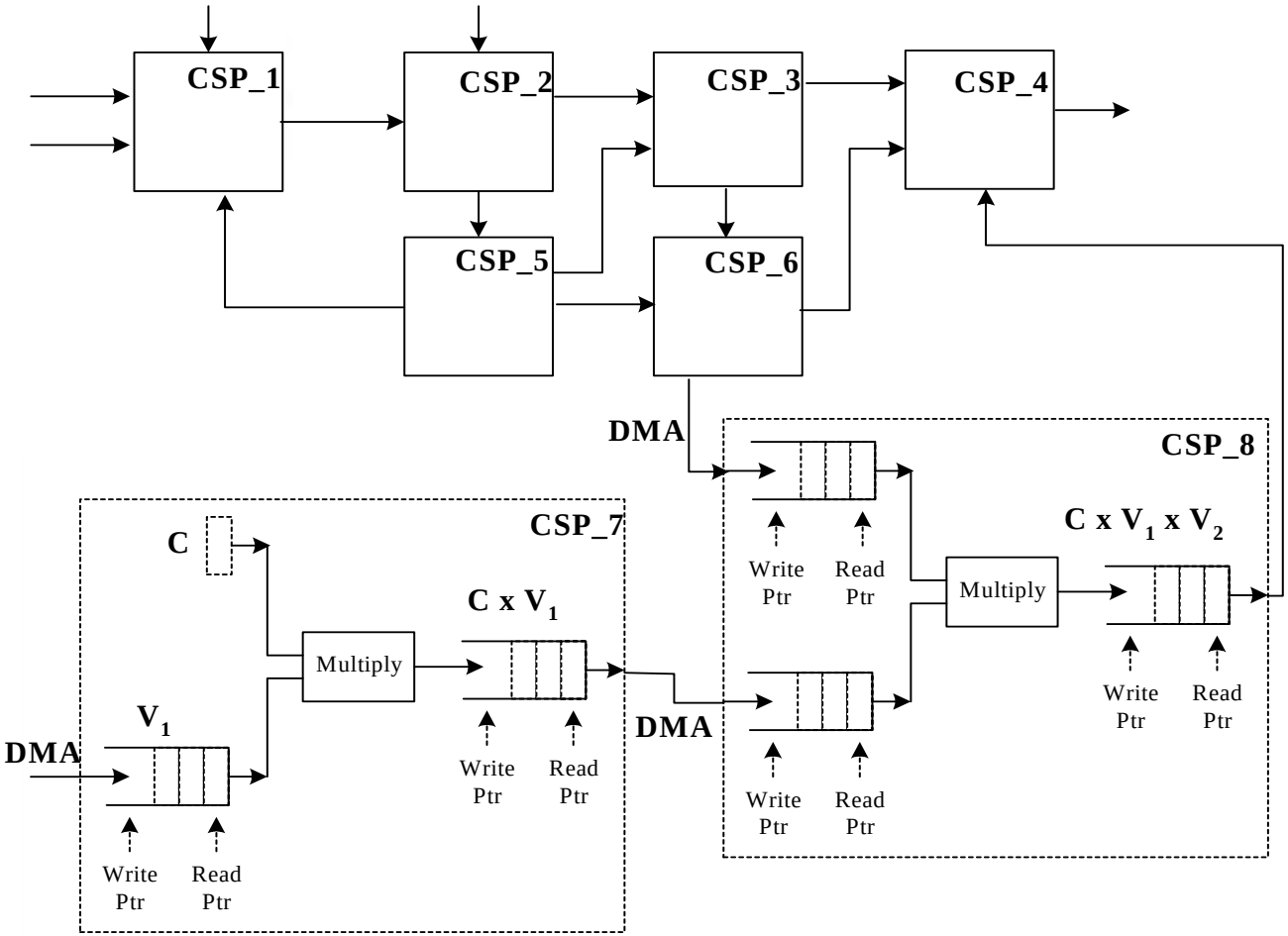
Programmable number of buffers - 1 to 16

- **Programmable buffer size – 128, 256, 512, 1K locations**
- **A *vector register (or, a vector)* is a portion of a buffer – vector length is programmable**
- **Vectors are accessed via vector instructions**
- **Implicit process synchronization - vector instruction will not start "on an empty vector"**



CSP Architecture

CSP Multiprocessing



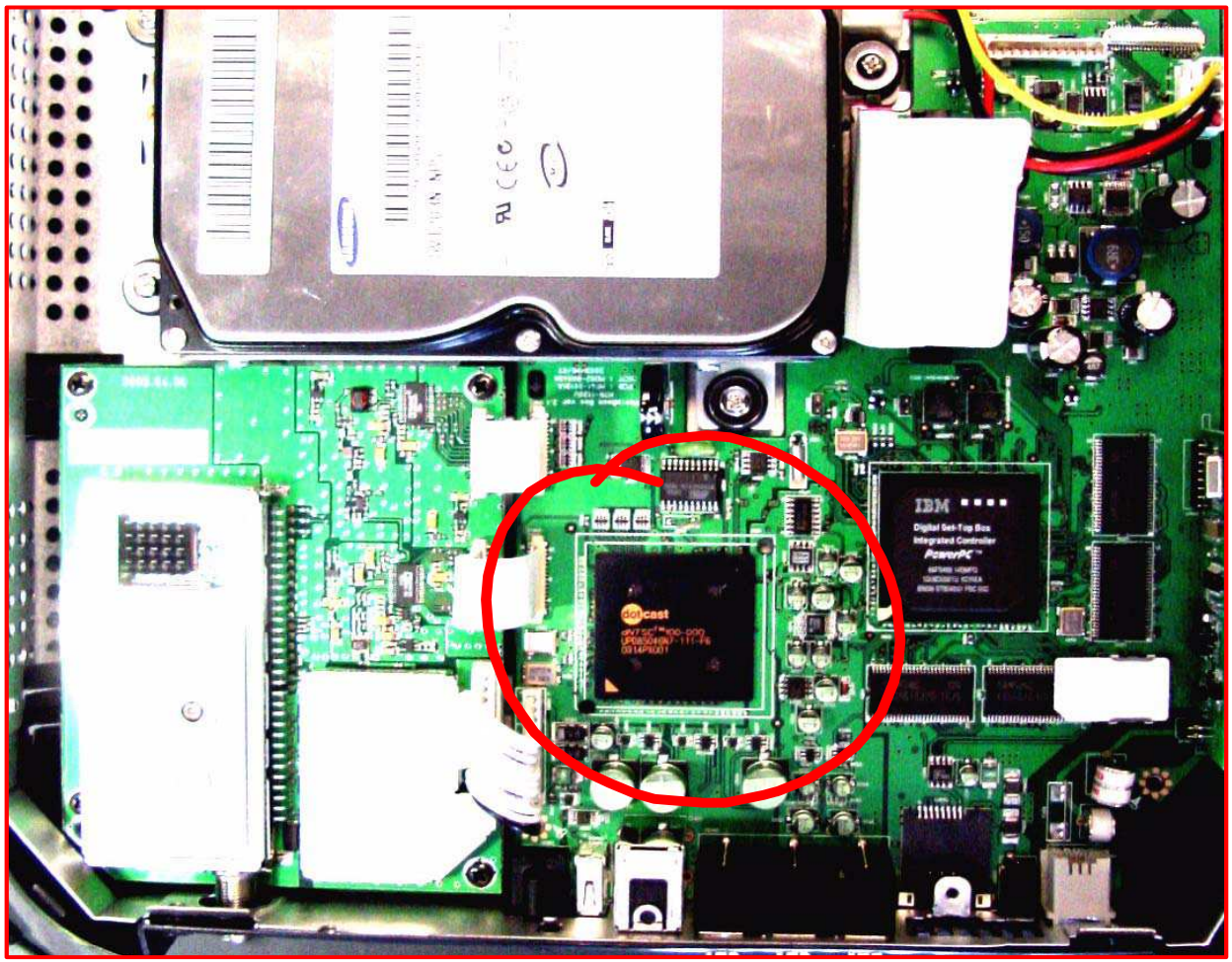
ReX Implementation

Vital statistics:

- 0.25 micron (NEC)
- 5 metal layers
- ~3M gates
- 12.5mm x 12.5mm
- 160MHz max freq
- 352TBGA package
- taped out: 12/02
- productized: 3/03
- in the box: 5/03
- in the field: 7/03

Applications of dNTSC™

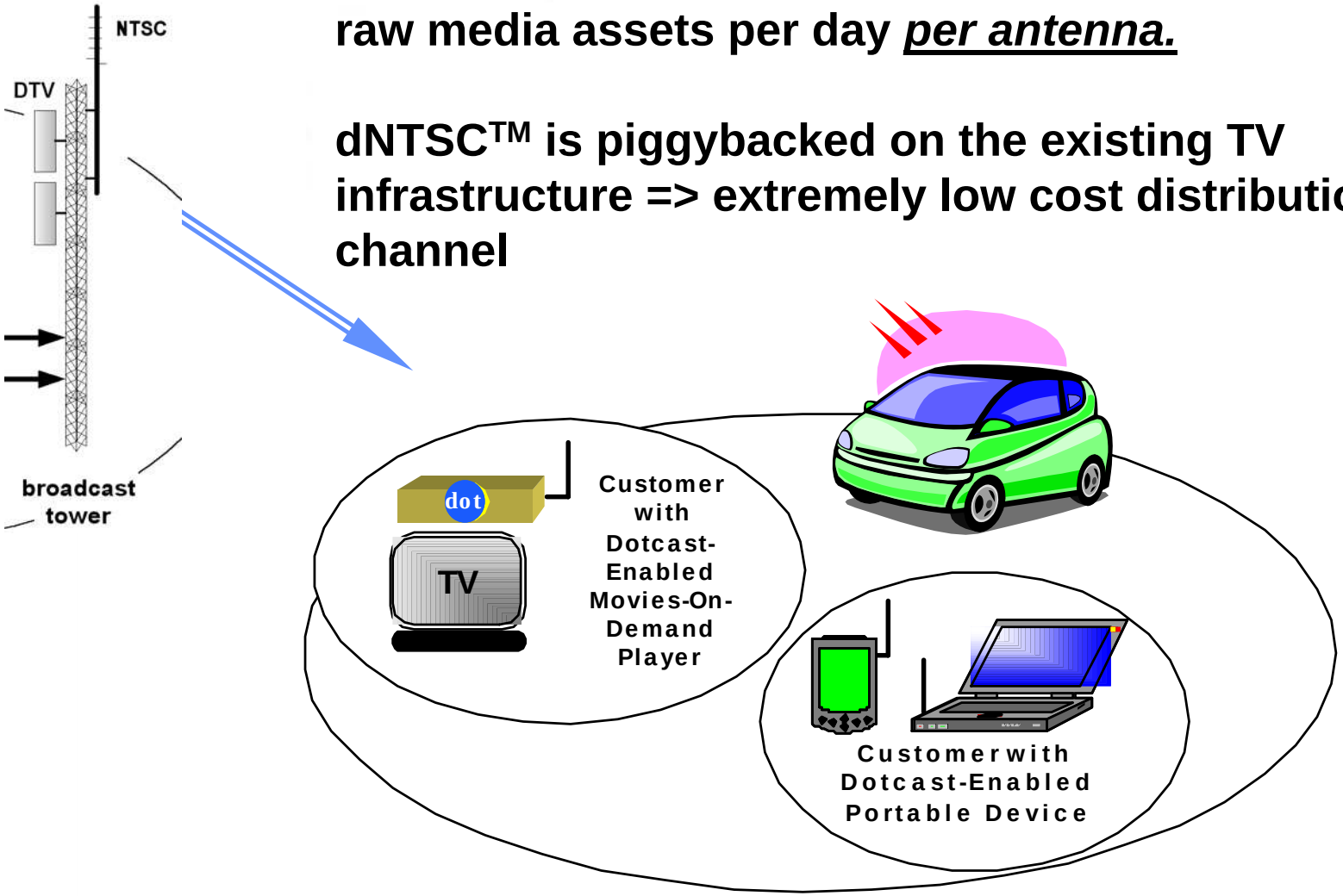
ReX-based wireless set-top box



Applications of dNTSC™

dNTSC™ broadcast pipe delivers over 25GByte of raw media assets per day *per antenna.*

dNTSC™ is piggybacked on the existing TV infrastructure => extremely low cost distribution channel



Summary

- dNTSC™ – technology for datacasting over analog NTSC television supporting up to 4.5Mbit/sec @ 10^{-8} BER within TV station's A contour
- ReX – first ASIC implementation of the dNTSC™ receiver technology supporting up to 3Mbit/sec over visual subcarrier
- dNTSC™ decoding algorithm implemented in ReX as a combination of dedicated- and fully-programmable processing elements (CSPs)
- Configurable Stream Processor (CSP) – general-purpose DSP core optimized for stream processing applications
- ReX productized and will be used in a consumer device scheduled for commercial deployment in 2003 – Disney's MovieBeam™ Service

www.dotcast.com

Dotcast Inc.
20425 72nd Avenue South, Suite 200
Kent, Washington 98032 U.S.A.
253-867-2000

email: info@dotcast.com