New 130nm Itanium® 2 Processors for 2003

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Intel Corporation, Santa Clara, CA
Outline

• Processor highlights
• Itanium® 2 processor evolution
• Block diagram
• Power dissipation
• Package details
• Front-side bus interface
• DFT and DFM features
• Performance details
• System level implementation
• Summary
Itanium® 2 Processor 6M Highlights

- 130nm process
- 410M transistors
- 374mm² die size
- 6MB on-die L3 cache
- 1.5GHz at 1.3V
- 6.4GB/s 400MT/s 4-way bus interface
- System compatible with existing Itanium 2 platforms
- Extensive RAS, DFT and DFM features

Largest microprocessor transistor count and on-die cache
Next generation platforms with advanced features planned for ’06 and beyond

Itanium® 2 Processor (Madison 9M)
>1.5GHz, 9MB

Montecito-based DP

Montecito Dual Core, Larger Caches, 90nm Technology

LV Itanium® 2 Processor (Deerfield Refresh) DP, Low Voltage

Deerfield Follow-on DP, Low Voltage

LV Itanium® 2 Processor (Deerfield) 1.0GHz, 1.5MB, DP

Itanium® 2 Processor (Madison 9M-based) DP

Itanium® 2 Processor (Madison) 1.5GHz, 6MB 1.4GHz, 4MB 1.3GHz, 3MB

Product Key
Multi-Processor Capable

Leading Performance

Dual Processor Capable

Leading $ / FLOP

Lower Power

†Low Voltage Intel® Itanium® 2 processor

All products, dates and information are preliminary and subject to change without notice
# Itanium® 2 Processor Evolution

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Itanium® 2 Processor</th>
<th>Itanium® 2 Processor 6M</th>
<th>Low Voltage Itanium® 2 Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code name</td>
<td>McKinley</td>
<td>Madison</td>
<td>Deerfield</td>
</tr>
<tr>
<td>Architecture</td>
<td>Explicitly Parallel Instruction Computing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Process</td>
<td>180nm</td>
<td>130nm</td>
<td>130nm</td>
</tr>
<tr>
<td>On-die L3 cache</td>
<td>3MB</td>
<td>6MB</td>
<td>1.5MB</td>
</tr>
<tr>
<td>Frequency</td>
<td>1.0GHz</td>
<td>1.5GHz</td>
<td>1.0GHz</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.5V</td>
<td>1.3V</td>
<td>1.1V</td>
</tr>
<tr>
<td>Max. Power</td>
<td>130W</td>
<td>130W</td>
<td>62W</td>
</tr>
<tr>
<td>Thermal Design Power</td>
<td>100W</td>
<td>107W</td>
<td>≤ 55W</td>
</tr>
<tr>
<td>Target market</td>
<td>MP servers, workstations</td>
<td>MP-servers, workstations</td>
<td>DP-servers, workstations</td>
</tr>
</tbody>
</table>
Thermal Design Power

- **Realistic** worst case application power
  - Based on various application loads
- Approx. 90% of theoretical max power (MPP)
  - MPP conditions are unrealistic for system applications
- Thermal Design Envelope (TDE) set at MPP level
  - Ensures system compatibility with future Itanium 2 processors

**Thermal Design Envelope**

- **2002**: 1.0GHz, 3M
- **2003**: 1.5GHz, 6M
- **2004**: >1.5GHz, 9M

**TDP**

- 130W
- 107W
- 100W

*Itanium® 2 Processor-based System*
Block Diagram

- **ECC protected**
- **Parity protected**

- **L3 Cache**
- **L2 Cache**
- **Branch Prediction**
- **L1 Instruction Cache and Fetch/Pre-fetch Engine**
  - Instruction Queue
  - ITLB
  - 8 bundles
- **Register Stack Engine / Re-Mapping**
- **IA-32 Decode and Control**
- **Quad-Port L1 Data Cache and DTLB**
- **Branch Units**
- **Integer and MM Units**
- **128 Integer Registers**
- **128 FP Registers**
- **Scoreboard, Predicate, NATs, Exceptions**
- **ALAT**
- **Floating Point Units**

Bus (128b data, 6.4GB/s @400MT/s)
Itanium® 2 Processor 6M Cache Summary

<table>
<thead>
<tr>
<th>Attribute</th>
<th>L1I</th>
<th>L1D</th>
<th>L2</th>
<th>L3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>16K</td>
<td>16K</td>
<td>256K</td>
<td>Up to 6M</td>
</tr>
<tr>
<td>Line Size</td>
<td>64B</td>
<td>64B</td>
<td>128B</td>
<td>128B</td>
</tr>
<tr>
<td>Ways</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>24</td>
</tr>
<tr>
<td>Replacement</td>
<td>LRU</td>
<td>NRU</td>
<td>NRU</td>
<td>NRU</td>
</tr>
<tr>
<td>Latency</td>
<td>1-Fetch:1</td>
<td>INT:1</td>
<td>INT: 5</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FP: NA</td>
<td>FP: 6</td>
<td></td>
</tr>
<tr>
<td>Write Policy</td>
<td>-</td>
<td>WT (RA)</td>
<td>WB (WA)</td>
<td>WB (WA)</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>R: 48GBs</td>
<td>R: 24GBs</td>
<td>R: 48GBs</td>
<td>R: 48GBs</td>
</tr>
<tr>
<td></td>
<td>W: 24GBs</td>
<td>W: 48GBs</td>
<td>W: 48GBs</td>
<td>W: 48GBs</td>
</tr>
</tbody>
</table>

- Compared to the original Itanium® 2 Processor:
  - Cache bandwidths increased by 50%
  - L3 size and set associativity doubled
140 subarrays tiled to fit irregular shape of core

4 subarrays/group, only 1 is active

8 bits/group/access

Physical Address Decoding:

Tag Address

Set Address

Byte Select

24-way set associative

direct-mapped

Subarray Address:

Way

Wordline

Block

Group

Column

Info

Info

Index

Index

Select
L3 Power Reduction Scheme

Previous Implementation

Index [4:3] == '11
Index [4:3] == '10
Index [4:3] == '01
Index [4:3] == '00

Bank 1 Request
Bank 0 Request

Data in [7:0]
Data out [7:0]

Two data bits per subarray
Index[4:3] enables 4 subarrays

This work

Index [4:3] == '11
Index [4:3] == '10
Index [4:3] == '01
Index [4:3] == '00

Bank 1 Request
Bank 0 Request

Data in [7:0]
Data out [7:0]

Eight data bits per subarray
Index[4:3] enables 1 subarray
Power

• Same thermal design envelope as the 180nm Itanium® 2 processor
  – 50% frequency increase
  – 2X larger L3 cache
  – Leakage increased 3.5X

Itanium® 2 Processor 3M (180nm)

- Dynamic power: 90%
- I/O power: 5%
- Leakage+static: 5%

Itanium® 2 Processor 6M (130nm)

- Dynamic power: 74%
- I/O power: 5%
- Leakage+static: 21%
Itanium® 2 Processor 6M Package Details

- Flip-Chip BGA package with Integrated Heat Spreader
- Interposer Substrate
- Power delivery connector
- Server Management Components
Package Decoupling

Vdd (core)
Vtt (FSB)
PLL filter

Power delivery connector
Front Side Bus

<table>
<thead>
<tr>
<th>Interface Support</th>
<th>Glueless 4-way Multi-Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Topology</td>
<td>Dual-sided board, staggered vias</td>
</tr>
<tr>
<td>Termination Voltage</td>
<td>1.2V, common ground with core</td>
</tr>
<tr>
<td>Voltage Reference</td>
<td>Ground-referenced, 0.75V Vref</td>
</tr>
<tr>
<td>Data Bus Width</td>
<td>128-bit</td>
</tr>
<tr>
<td>Data Bus Speed</td>
<td>400MT/s source synchronous</td>
</tr>
<tr>
<td>Data Strobes</td>
<td>1 differential strobe for 16b of data</td>
</tr>
<tr>
<td>Peak BW</td>
<td>6.4GB/s</td>
</tr>
<tr>
<td>Address, Control Speed</td>
<td>200MHz common clock</td>
</tr>
</tbody>
</table>
Front-Side Bus Topology

Previous implementation
Four linear stripes

This work
U-shape

Core

L3 Cache

Core

L3 Cache

Data I/O
Address I/O
Control I/O
# DFT/DFM Feature Summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>Itanium® Processor</th>
<th>Itanium® 2 Processor</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scan Coverage</td>
<td>48K</td>
<td>140K</td>
<td>140K</td>
</tr>
<tr>
<td>Scanout Coverage</td>
<td>5.5K</td>
<td>24K</td>
<td>24K</td>
</tr>
<tr>
<td>Cache DAT Mode (major arrays)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>L3 Redundancy / Repair</td>
<td>N/A</td>
<td>Dual</td>
<td>Quad</td>
</tr>
<tr>
<td>Weak-Write Test Mode</td>
<td>Fixed</td>
<td>Fixed</td>
<td>Programmable</td>
</tr>
<tr>
<td>IO DFT</td>
<td>Basic IO Loopback</td>
<td>Limited IO Loopback</td>
<td>Enhanced IO Loopback</td>
</tr>
<tr>
<td>Dynamic Frequency Adjustment</td>
<td>Multi-cycle shrink/stretch</td>
<td>Single cycle shrink/stretch</td>
<td>Multi-cycle shrink/stretch</td>
</tr>
<tr>
<td>On-die process monitors</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Itanium® 2 Processor 6M: Industry Leading Performance Results vs. Best RISC

Results as of 6/23/03.

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Best RISC Result</th>
<th>Industry Leading Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint_base2000</td>
<td>1322</td>
<td>2119</td>
</tr>
<tr>
<td>SPECfp_base2000</td>
<td>1P</td>
<td>4P</td>
</tr>
<tr>
<td>TPC-C</td>
<td>121K tpmC</td>
<td>$4.97/tpmC</td>
</tr>
<tr>
<td>SAP</td>
<td>860 SD Users</td>
<td>1873</td>
</tr>
<tr>
<td>SPECweb_SSL</td>
<td>116K</td>
<td>156 GFLOPS</td>
</tr>
<tr>
<td>SPECjbb</td>
<td>707K tpmC</td>
<td>$9.13/tpmC</td>
</tr>
</tbody>
</table>

With Same Number of Processors

1. SPECint_base2000: Itanium® 2 processor results measured on HP Server rx2600 using Itanium® 2 processor 6M at 1.5GHz, HP-UX operating system and submitted to SPEC. SPECint® is a trademark of SPEC®. Best RISC result of 1077 on eServer pSeries IBM 690 using Power4+ 1.7GHz processor.
2. SPECfp_base2000: Itanium® 2 processor results measured on HP Server rx2600 using Itanium® 2 processor 6M at 1.5GHz, RedHat Linux AS2.1 operating system and submitted to SPEC. SPECfp® is a trademark of SPEC®. Best RISC result of 1598 on eServer pSeries IBM 690 using Power4+ 1.7GHz processor.
5. SPEC: Itanium® 2 processor results published on HP Server rx6670 using 4 Itanium® 2 processors 1.5GHz with 6MB L3 cache, 12GB memory, HP-UX, Zeus 4.2r2, published 5/03. Best RISC result on Sun Fire® 280R processor of 1008 with 2 UltraSPARC® III Cu processors at 1.2GHz with 8MB L2 cache (off chip), Solaris® 9, Sun ONE Web Server 6.0 SP5, 32GB RAM, published 4/03.
6. SPECjbb: For Best published RISC result of 96,377 on eServer pSeries IBM 655 using 4 Power4+ 1.7GHz processors, 16GB memory, AIX 5L V5.2 APAR Y45549, JVM 1.4.1 IBM AIX build dated 2003/04/10. Itanium® 2 processor 6M result of 116,466 measured by HP on HP Server rx6670 using 4 Itanium® 2 processors 6M at 1.5GHz with integrated 6MB L3 cache, 4GB of memory, HP-UX 11i v2.2, JVM Hotspot 1.4.2.0 and submitted to www.spec.org. SPECjbb® is a trademark of SPEC at www.spec.org.
7. SPECweb: Dell Computer for Itanium® 2 processor 6M results on a cluster of 16 Dell PowerEdge Servers, each with 2 Itanium® 2 processors 6M at 1.5GHz, 4GB RAM, RedHat Linux AS 2.1. Source: http://www1.ibm.com/servers/eserver/serverproven/hardware/system_perf.pdf for Best RISC result of 143,3GFLOPS on IBM eServer p690 with 32 Power 4+ processors at 1.7GHz.
8. SPECjbb: For Best published RISC result of 96,377 on eServer pSeries IBM 655 using 4 Power4+ 1.7GHz processors, 16GB memory, AIX 5L V5.2 APAR Y45549, JVM 1.4.1 IBM AIX build dated 2003/04/10. Itanium® 2 processor 6M result of 116,466 measured by HP on HP Server rx6670 using 4 Itanium® 2 processors 6M at 1.5GHz with integrated 6MB L3 cache, 4GB of memory, HP-UX 11i v2.2, JVM Hotspot 1.4.2.0 and submitted to www.spec.org. SPECjbb® is a trademark of SPEC at www.spec.org.

Results as of 6/23/03.

Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, reference www.intel.com/proc/perf/limits.htm or call (U.S.) 1-800-628-8686 or 1-916-356-3104.
Itanium® 2 Processor 6M at 1.5GHz:
Delivering on the promise of 30-50% performance improvement over
Itanium® 2 Processor 1GHz

<table>
<thead>
<tr>
<th>Test</th>
<th>Itanium® 2 Processor 1GHz</th>
<th>Itanium® 2 Processor 6M at 1.5GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint*_base20001</td>
<td>1P</td>
<td>1P</td>
</tr>
<tr>
<td>SPECfp*_base20002</td>
<td>1P</td>
<td>1P</td>
</tr>
<tr>
<td>TPC-C3</td>
<td>4P</td>
<td>4P</td>
</tr>
<tr>
<td>SAP 2-tier SD4</td>
<td>4P</td>
<td>4P</td>
</tr>
<tr>
<td>SPECweb99_SSL5</td>
<td>2P</td>
<td>2P</td>
</tr>
<tr>
<td>Linpack HPC6</td>
<td>32P</td>
<td>32P</td>
</tr>
</tbody>
</table>

1 Source: www.spec.org: Itanium® 2 processor 6M results measured on HP Server rx2600 using Itanium® 2 processor 6M at 1.5GHz, HP-UX operating system and submitted to SPEC. SPECint* is a trademark of SPEC*. Itanium® 2 processor result of 810 measured on HP Server rx2600 using Itanium® 2 processor 1GHz with integrated 3MB L3 cache, HP-UX operating system.

2 Source: www.spec.org: Itanium® 2 processor 6M results measured on HP Server rx2600 using Itanium® 2 processor 6M at 1.5GHz, RedHat Linux AS2.1 operating system and submitted to SPEC. SPECfp* is a trademark of SPEC*. Itanium® 2 processor result of 1431 on HP Server rx5670 using Itanium® 2 processor 1GHz with 3MB L3 cache, RedHat Linux 2.1.


5 Source: www.spec.org: Itanium® 2 processor 6M result of 1873 on HP Server rx2600 using 2 Itanium® 2 processors 1.5GHz with integrated 6MB L3 cache, 12GB memory, HP-UX, Zeus 4.2r2, published 5/03. Itanium® 2 processor result of 1230 on HP Server rx2600 using 2 Itanium® 2 processors 1GHz with 3MB L3 cache, 8GB memory, HP-UX, availability 9/02.

6 Source: Dell Computer for Itanium® 2 processor 6M results on a cluster of 16 Dell PowerEdge Servers, each with 2 Itanium® 2 processors 6M at 1.5GHz, 4GB RAM, RedHat Linux AS 2.1. Itanium® 2 processor measurement of 101.77GFLOPs done on a NEC Server TX7/i9510 using 32 Itanium® 2 processors 1GHz with integrated 3MB L3 cache, 128GB memory, Linux OS.

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Low Voltage Itanium® 2 Processor

• Extension of the Itanium® processor family
  – 1.0 GHz, 1.5 MB L3 cache, DP/UP only
  – 62W maximum power, over 50% lower than Itanium® 2 processor 6M
  – Compatible with Itanium® 2-based DP platforms

• Target market
  – Entry 64-bit servers and performance workstations
  – High density form factors benefit from lower power
  – Application segments including security, application development network edge and HPC

• Schedule
  – Platform release target: Q3 2003

Performance similar to Itanium® 2 processor 1.0GHz at about half the power

Sources: Sun* and Alpha* - <www.spec.org>; Intel - Intel pre-production estimates for Low Voltage Itanium® 2 processor.
## Intel 2 and 4-way System Configurations

<table>
<thead>
<tr>
<th>Feature</th>
<th>SR870BN4 (Tiger-4)</th>
<th>SR870BH2 (Tiger-2)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Rack Units</strong></td>
<td>4U</td>
<td>2U</td>
</tr>
<tr>
<td><strong>Processor</strong></td>
<td>Intel® Itanium® 2 processor</td>
<td></td>
</tr>
<tr>
<td><strong>Chipset</strong></td>
<td>Intel® E8870</td>
<td></td>
</tr>
<tr>
<td><strong>Memory Capacity</strong></td>
<td>32GB in 16 DIMMs</td>
<td>16GB in 8 DIMMs</td>
</tr>
<tr>
<td><strong>PCI Slots</strong></td>
<td>8 PCI-X</td>
<td>3 PCI-X</td>
</tr>
<tr>
<td></td>
<td>3 @ 133 MHz</td>
<td>1 @ 133 MHz</td>
</tr>
<tr>
<td></td>
<td>5 @ 100 MHz</td>
<td>2 @ 100 MHz</td>
</tr>
<tr>
<td><strong>HDD Capacity</strong></td>
<td>3 HDDs, 220GB</td>
<td>2 HDDs, 145GB</td>
</tr>
<tr>
<td><strong>On-board Ethernet</strong></td>
<td>Single Kenai32</td>
<td>Dual Anvik</td>
</tr>
<tr>
<td><strong>Graphics</strong></td>
<td>ATI* Rage* XL VGA</td>
<td>ATI* Rage* XL VGA</td>
</tr>
<tr>
<td><strong>Cooling</strong></td>
<td>(4) fans = (2) 1&quot; + (2) 1.5&quot; redundant &amp; hotswap</td>
<td>(6) fans redundant &amp; hotswap</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>(2) 1200W TPS, hot-swap 1+1 redundant</td>
<td>(3) 350W TPS, hot swap 2+1 redundant</td>
</tr>
</tbody>
</table>
Madison 9M Key Features

- Itanium® 2 platform compatibility
- Socket and system bus compatible
- Shares the same chip set
- Binary compatible with Itanium® processor software
- Increase L3 cache size to 9MB on 130nm process
- Increase frequency above 1.5GHz
- Also refresh “DP only” Itanium® 2 processor offerings
Summary

• The Itanium® 2 Processor 6M (Madison) delivers 2X larger on-die cache and 50% higher frequency
• Compatible with today’s Itanium® 2-based systems
• Enterprise-class RAS, DFT and DFM features
• Largest on-die cache and transistor count ever reported for a microprocessor
• Low Voltage Itanium® 2 processor to deliver performance similar to Itanium® 2 processor 1.0GHz at about half the power
• Itanium roadmap committed to delivering leading performance through innovation