Terabit Clockless Crossbar Switch in 130nm

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Nexus Silicon Validation Chip Project

**Chip characteristics**

- 16-port asynchronous crossbar
- 1.4 GHz (effective frequency)
- 1.6 Tbps capacity (aggregate)
- >400 Gbps / Watt (aggregate)
- <3ns latency (+ target clock)
- 1.75mm² (crossbar size)
- 7 independent clock domains

**Project details**

- Semi-custom async design flow
- 6-month effort (start to tape-out)
- ~1M transistors (500K in Nexus)
- Standard 130nm fab process
Agenda

• Introduction to Fulcrum

• Description of Integrated Pipelining
  - Fulcrum’s clockless circuit architecture

• Review of Nexus
  - Fulcrum’s Terabit crossbar

• Introduction to PivotPoint
  - Fulcrum’s first commercial product
Company Snapshot

“Clockless”
Semiconductor Company

Formed out of Caltech
(1/00)

Technology proven
in large-scale designs

Located in Calabasas, CA
(30 people)

Backed by top-tier investors
(raised $14M in June)

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Fundamental Mode (The Beginning)

Race conditions led to the addition of the latch

Predates invention of the clock (combinational logic with feedback)
Clock and Latches Introduced

Circuits became predictable, enabling larger designs

Predominant design style for several decades
Bundled Data (Micro Pipelines)

Delay element tuned to each logic block

Synchronous-style data path; asynchronous channels
(Ivan Sutherland, Sun Labs)
Delay-Insensitive (Traditional)

Robust and low power, but also large and low performance

Dynamic logic; similar number of N and P transistors; separate latches
(Early MIT and later Caltech research)
Fulcrum’s Integrated Pipelining

Robust, power efficient, and high performance

Fast delay-insensitive style using domino logic without latches
(Developed at Caltech by Fulcrum’s founders)
Integrated Pipelining

- Harnessing the power of Domino Logic
  - Addresses delay variability with Completion Sensing
  - Addresses power inefficiency with Asynchronous Handshakes
  - Leverages more efficient “N” transistors
The Advantages of Asynchronous

- **High performance (cycle-time efficient)**
  - Cycle time of clocked logic
  - Cycle time of clockless logic
  - Logic Time
  - Manufacturing margin
  - Clock jitter, skew margin
  - Worst case – average case (logic execution time)

- **Power efficient**
  - No clock tree
  - No wasted logic transitions – perfect clock gating

- **Robust**
  - Wide operating range of temperature and supply voltage

- **High integration**
  - Eases the transition between multiple clock domains
(Perceived) Disadvantages

• **Limited commercial tool support**
  - Migrating to commercial tools; partnered with tools providers

• **Additional wires**
  - Feasible in modern fabrication processes

• **Area overhead**
  - Comparable to high-speed synchronous overhead
  - Excellent throughput/area
Fulcrum Design Flow

- Hierarchical design flow
  - Executable specifications
  - Formal decomposition
  - Creates design hierarchy

- Semi-custom synthesis & layout
  - Hierarchical floor planning
  - Automated transistor sizing
  - Semi-automated physical design

- Supports synchronous & asynchronous designs
  - Hard macro from place & route
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Nexus System-on-a-Chip Interconnect

- Non-blocking crossbar
- 16 full-duplex ports
- Self-queuing ports extend through the crossbar
- Line rate arbitration
- Arbitrary-length “bursts”
- Seamlessly bridges between clock domains
- Scales in bit width and ports
- Process independent

Generic Nexus Example

- Synchronous IP block
- Asynchronous IP block
- Pipelined repeater
- Clock domain converter
Nexus Burst Format

Arbitrary-length source-routed bursts provide system flexibility

Incoming From Source

- Data: 36 bit
- Tail: 1 bit
- Control: 4 bit

Outgoing To Target

- Data: 36 bit
- Tail: 1 bit
- Control: 4 bit
Nexus Validation Chip (TSMC 130nm)

- **High capacity**
  - 1.6 Tbps aggregate b/w
  - 800 Gbps cross-section b/w

- **Low latency**
  - Less than 3ns (+ target clock)

- **Power efficient**
  - > 400Gbps per Watt (aggregate)
  - Scales linearly with activity
  - Zero standby power

- **Area efficient**
  - 1.75mm² (crossbar)
  - 2mm² (converter & repeaters)

- **Fabrication process:**
  - TSMC 130nm LowK
    - 25mm² shuttle
  - Also fab’d in TSMC 130nm FSG
    - 25mm² shuttle
Predictable Operation Over Voltage

1.4GHz at nominal voltage (1.2V)

(TSMC 130nm LowK and FSG processes)
Robust Operation Over Temperature

*Predictable operation from -55°C to 125°C*

(TSMC 130nm LowK and FSG processes)
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Introducing PivotPoint Blade Interconnect

World’s first high-performance clockless chip

• Large-scale SoC design
  - >32.5M transistors (83% async)
  - 14 separate clock domains

• Includes key Fulcrum IP
  - Nexus Terabit Crossbar
  - Quad-port 600MHz async SRAM

• Operates at over 1GHz

• Delivers 192Gbps of non-blocking switching capacity

• Testable via standard tools
  - JTAG; scan chain

• Activity-based power scaling

• 9-month project
Systems have outgrown the effective capacity of the bus

- System performance bottlenecked by bus-based interconnect
  - Bus electricals inadequate for today’s high-speed designs
  - Traditional load/store model inefficient for streaming data
Today’s Problem: No Hardware Flexibility

Fixed-configuration solutions limit configuration flexibility

- Solution to bus-based problems
- Creates new architecture problems:
  - Inefficient use of in-line devices
  - Sharing ingress and egress resources is prohibited
PivotPoint Eliminates Deficiencies

**Creating soft-configurable pool of resources**

- **High performance**
  - Low latency
  - High capacity
  - Sophisticated flow control

- **Highly flexible**
  - Fully programmable
  - Any-to-any connectivity
  - Source routing; channel switching

- **Low cost**
  - Fewer blade variants required
  - Lower per-unit cost than FPGAs
  - Lower design cost than ASICs

- **Power efficient**
  - Low power profile
  - Power scales linearly on activity
An Illustration of Complex Flows

Supports complex flows through channel assignment

1. Packet is delivered to NPU on configured SPI-4.2 channel
2. NPU parses packet, determines the packet is encrypted, and sends the packet to the security processor by assigning it a new SPI-4.2 channel
3. Security processor decrypts the packet and sends it back to the NPU for additional processing, assigning it a different SPI-4.2 channel
4. NPU completes its work on the packet and sends it out on a new SPI-4.2 channel
5. PivotPoint re-assigns the packet to the original SPI-4.2 channel and sends it out
Low-Cost Multi-Gigabit Router

PivotPoint supports high-capacity routing

• NPUs classify packets, identify destination, and assign appropriate SPI-4 channel
• PivotPoint routes based on SPI-4 channel
PivotPoint Leverages Nexus

A true SoC GALS design

- **Flexible architecture**
  - 6 duplex SPI-4.2 interfaces
  - All paths are independent

- **Optimized for performance**
  - Up to 14.4Gbps per interface
  - Up to 32Gbps per Nexus port
  - Full-rate buffer memories
  - Lossless flow control

- **Easily configurable**
  - 16-bit CPU interface
  - JTAG support

- **Modest size and power**
  - ~2 Watt per active interface
  - 1036 ball package
The Future of PivotPoint

Efficiently link the data plane with the “midplane”

Control Plane
System-level control, configuration, exception handling, and monitoring

“Midplane”
With PivotPoint at the heart, the midplane features all of the software-driven intelligence for layer 4-7 services

Data Plane
Organized for high-speed packet parsing and forwarding
Differentiating Through Technology

Leveraging our clockless technology foundation

**Differentiated Product Offering**
- High performance (latency, capacity)
- Power efficient (linear scaling)
- Robust in operation

**Unique IP Blocks**
- Unmatched performance
- Extremely robust (power and temperature)
- Easy to integrate (benign behavior)

**Clockless Technology Foundation**
- Silicon proven and customer validated
- Mature CAD flow (integrated with commercial tools)
- Robust cell library (thousands of unique cells)
“A group of engineers wants to turn the microprocessor world on its head by doing the unthinkable: tossing out the clock and letting the signals move about unencumbered. For those designers, inspired by research conducted at Caltech, clocks are for wimps.”

Anthony Cataldo, EE Times