output Adaptive Packet Processor (oAPP)

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oAPP – output Adaptive Packet Processor
oAPP – Shipping in PRO/8000 series

PRO/8801

PRO/8804

PRO/8812
oAPP – Agenda

oAPP
- Features
- Top-Level
- Blocks
- Design challenges
- Design flow
- Q & A

PRO/8812
- System
- Architecture
- Key concepts
PRO/8812 – System

- 2 DC Power Entry Modules
- 2 Route Processors
- 3 Switch Cards
- 12 40Gbps Line Cards
- 48 10Gbps Media Adapters
- Air Filter
- 2 Fan Assemblies
• iAPP and oAPP on Linecard
• 4 Media Adapters (MAs) plug into Linecard
• iAPP performs input processing
• oAPP performs output processing
oAPP

High performance
• 40 Gbps
• Non-blocking
• Traffic Management
• Encapsulation

Programmable
• QoS
• Encapsulation

Fully featured
• Shaping
• Accounting
• QoS
• Multicast
• Fragmentation

Robust
• OIR
• BIST
• ECC/parity
• CRC24

Design challenges
oAPP – High Performance

Active Switchcard (A)

Inactive Switchcard (B)

Active Switchcard (C)

Counters SRAM

Multicast SRAM

40 Gbps MAs

Flow-control from MAs
oAPP – Fully Featured

Cell Notifications

- Interface
- Q Selection

Cell Requests

- Interface
- Packet Scheduler
- Engine Scheduler

Buffer

Cells

Packet Scheduler

Engine Scheduler

Encapsulation Engines

Assemblers

MA
MA
MA
MA
oAPP – Fully Featured

• Accounting
  • Precise packets and bytes
  • Per port
  • RED drops
  • Metering drops

• Multicast replication

• Fragmentation
oAPP Programmable – Queue Selection

- Queue and group-queue rate-shaping
- Selectable per interface
- Disciplines currently programmed:

- **STRAIGHT PRIORITY**
  - High Priority
  - Low Priority

- **DWRR**
  - Equal Priority
  - 5% 18% 47% ...

- **PRIORITY DWRR**
  - High Priority
  - | A | B | C |
  - | 90% | 10% | 40% ... 27% 34% |

- **DWRR PRIORITY**
  - 70% 18% 12%
**oAPP Programmable – Encapsulation Engines**

- **Multiple Encapsulation Engines**
  - Fully programmable
  - Easily add new encapsulations

- **Encapsulation engine**
  - Modifies packet
  - L2 encapsulation
  - Physical port identifier
  - Send cells to Assembler
oAPP Robustness – Switchcard Failover

- **Active Switchcard (A)**
- **Inactive Switchcard (B)**
- **Active Switchcard (C)**

To MAs

State for SC A

State for SC B
oAPP Robustness – Reliability

- ECC/parity
  - On-chip SRAM
  - Off-chip SRAM
- BIST & repair
- End-to-end packet CRC-24
- Inter-chip
  - CRC
  - Parity
  - ECC
- Internal consistency checks
oAPP Design Challenges

- **Speed**
  - 40Gbps
  - 100+ Mpps
  - 350 MHz
  - 0.18um copper CMOS

- **Scale**
  - Programmable engines
  - 950KBytes SRAM
  - 137M transistors
  - 425 sq mm

- **Analog**
  - 170 2.5 GHz serial links
  - Multiple clock domains
  - Power
oAPP Design Challenges – ASIC

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oAPP Design Challenges – COT

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  - 170 2.5 GHz serial links
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  - Power efficient
oAPP Design Challenges – COT
oAPP – Summary

High Performance
Shipping
Robust
Programmable
Full-Featured
High Performance
COT

PRO/8801
PRO/8804
PRO/8812
<table>
<thead>
<tr>
<th>Procket VLSI Development</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VLSI IP &amp; Expertise</strong></td>
</tr>
<tr>
<td>System/Chip Architecture</td>
</tr>
<tr>
<td>Design/Verification</td>
</tr>
</tbody>
</table>

VLSI Services
2.5 GHZ Serial Links in 0.18 and 0.13 um

- Source synchronous
- Very low BER
- 48 inches backplane trace + 2 connectors
- Multilink bundling
- Low power (<200mW in 0.18 um)
- oAPP has 170 links – other Procket chips more than 250
Procket VLSI Development

VLSI IP & Expertise

System/Chip Architecture  Design/Verification  Serial Link  SRAM

High-performance embedded SRAM

• Creation of any configuration
• 500MHz designs achieved in 0.18
  • 2-port and 4-port
• Row/column redundancy
  • RAMBist design for test and reliability
Procket VLSI Development

VLSI IP & Expertise

- System/Chip Architecture
- Design/Verification
- Serial Link
- SRAM
- Libraries

Standard-Cell and IO Library Design

- High speed/low power FFs
- Automated RTL to I/O Frame generation
- Proprietary clock distribution
  - reduced power and clock skew
Packaging

- *Flip-Chip CGA, HITCE glass ceramic*
  - 16 GHz bandwidth
  - 58 mm. Body size
  - 20 layers
- *HiTCE improves reliability*
- *In-house automated design*
Procket VLSI Development

VLSI IP & Expertise

System/Chip Architecture  Design/Verification  Serial Link  SRAM  Libraries  Packaging

Backend/P&R:
- Customize around standard tools
- Internal development where necessary
- Custom clock distribution
- RTL freeze to GDS TO in 2 weeks!
- ECO acceptance 2 days before GDS TO
# Procket VLSI Development

## VLSI IP & Expertise

<table>
<thead>
<tr>
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</tr>
</thead>
</table>

## Test & Product Engineering

- **DFT methodology**
  - Highest test and fault coverage
- **High speed tests at wafer and module**
  - Process
  - Automated test vector translation
  - VLSI and product qualification
  - Burn-in and ESD tests
  - Delay and transition fault speed sorting
# Procket VLSI Development

## VLSI IP & Expertise

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## Process/Yield Enhancement

- Yield calculation/enhancement and FA
- Tune process
- Bit mapping and analysis of all RAMs
- Process/speed monitoring
- Data correlation
- Yield tracing
oAPP – Procket VLSI COT Development

VLSI IP & Expertise
- System/Chip Architecture
- Design/Verification
- Serial Link
- SRAM
- Libraries
- Packaging

VLSI Services
- Backend/P&R
- Test & Product Eng.
- Process/Yield Enhancement

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