Ubicom’s MASI Wireless Network Processor

David Fotland, CTO
Ubicom
http://www.ubicom.com
Ubicom Handles Packet Processing

- IP Routing
- Security
- Configuration & Management
- User Interface (Web, CLI)
- Protocol Translations
Traditional Architectures

- Running Linux or VxWorks demands large off-chip memory
- Off-chip memory forces caches, MMU and high-speed buses
- Large die area for dedicated hardware I/O that supports only one protocol at a time
- Above results in large die size and cost
Ubicom – Architected for Lowest Possible Cost

Software I/O
Small memory footprint
On-chip memory
¼ silicon area
Why MASI?

- Multithreaded Architecture for Software I/O
  - Over 75% of Communication SOC is I/O hardware
  - Increased I/O flexibility – one chip vs many
  - Deterministic hardware multithreading – thread per I/O port

- Efficient packet processing
  - Memory to memory for fast data movement and scanning
    - 2x to 4x faster than ARM or MIPS
  - Powerful bit manipulation (extract, merge, double shift)
  - Operate on packets directly in on-chip memory

- Increased code density
  - GCC-3.4, -Os (os, ethernet, tcp/ip, ppp, snmp, smtp, web)
  - IP3023: 67 KB (will get better as compiler matures)
  - ARM9: 69 KB
  - MIPS4K: 77 KB
Small, Powerful Instruction Set

- 16 data registers (Dn), 8 address registers (An), 32 bits each
- General Destination <= General source op Dn
- Operands: Register, 8-bit Immediate or Memory (8/16/32 bit)
- Addressing: An+Dn, An+immediate (optional increment)
- PC relative conditional branch. No delay slot
- 41 instructions
IP3023 Super-Pipeline: Higher Frequency

- 10-stage super-pipeline, single-cycle throughput
- Multi-threading hides branch penalty
  - Deep pipeline doesn’t hurt cycles per instruction
- Multi-threading adds a schedule stage
- Memory to memory adds 3 stages (Address, Read1 & Read2)
- Non-stalling pipeline. Independent thread timing
- No load-use penalty. Move An-Use An penalty instead.
- LEA and MOVAI bypass to avoid An hazard
Deterministic Multi-threading

• Up to 32 (architecture) simultaneous threads
  − Effectively operates as independent processors (non-blocking)
  − Each thread has its own registers
  − Processor is shared for most efficient utilization
  − Programmable instead of fixed-function

• Hard real-time threads (HRT) scheduled deterministically
  − One HRT thread per software I/O
  − Idle clocks available for NRT threads

• Non-real-time threads (NRT) scheduled round robin

• Suspend, setcsr instructions control threads
• Interrupt conditions unsuspend threads

• Zero cost context switch, every clock
• Deterministic branch prediction and memory latency
  − 1000x better interrupt latency (20 ns vs 20,000 ns)
  − Interrupt per word vs Interrupt per packet
IP3023 Chip Overview

• Ubicom instruction set architecture
• 8 simultaneous threads (typically 3 OS, 5 software I/O)
• Culmination of nearly 5yrs work on Software I/O
• On-chip 256 KB code & 64 KB data memory
  – No caches or cache misses
  – Smaller, simpler SDRAM memory controller
  – Fewer pins, lower power
  – ipOS + Stack under 100 KB
• 250 MIPS at 250MHz operation
• Power Management:
  – Core and I/O PLLs, clock divider, Sleep to 0.3 MHz
• Low-cost 208 PQFP package
IP3023 Block Diagram

32-Bit CPU CORE
Deterministic, multi-threaded, memory-memory

- SPI Debug
- CPU PLL
- Peripheral PLL
- Watchdog Timer
  - Reset & Brown-out
  - True Random Number Generator

- 256 KByte SRAM Program Memory
- 64 KByte SRAM Data Memory

- External 8-bit FLASH (2 MIPS)
- External 16-bit SDRAM 100 MB/s
- 4x MII GPIO
- Memory controller
- Parallel I/O
- Serial I/O
- 10BT USB SPI GPSI UART
IP3023 Additional Functions

- Hardware true-random number generator
  - 32-bit seed number for secure encryption keys
- CRCGEN instruction for CRC and scramblers
- 16-bit fixed point multiply/accumulate
  - Security and voice codecs
- Watchdog timer
- Multifunction timers
- Software I/O clock generator
- Powerful debug support
  - Break, single step, wild write detection, misaligned detection
  - 4 pin SPI interface with Ethernet dongle for remote debug
IP3023

- TSMC 0.13u G process
- 10-20 MHz crystal with on-chip multiplying PLLs
- 6.4 mm x 4.1 mm, 26 mm^2 die size
- 3.3V I/O (5V tolerant)
- 1.2V core power (+- 5%)
IP3023 Memory Structure

- 256 KByte on-chip code/packet memory
- 64 KByte on-chip data memory
- External Flash port, single 8-bit part, up to 4 MByte
  - Copy at boot with decompression in software
  - Direct execution at 2 MIPS for code expansion
- External SDRAM port, single 16-bit part
  - Copy to internal code or data memory, 100 MB/s
  - Not required for most applications
IP3023 I/O Ports

- 2 serializer/deserializer ports (or 8 GPIO each)
  - USB 1.1 master or slave, 10BT Ethernet, GPSI, SPI, UART
  - Bluetooth radio, 802.11b baseband interfaces
  - One on-chip 10BT PHY

- 4 MII ports (or 16 GPIO each)
  - Supports 10/100 PHY, HomePlug PHY, etc
  - Supports Phy-side MII for host connection

- 8 bit Flash & 16 bit SDRAM interface

- GPIO (106 maximum)
  - Pure software I/O

- In-system programming/debug port
IP3023 Software I/O

- Cardbus/PCI host: 802.11a, 802.11g (48 GPIO)
  - 25% HRT, 12 MIPS for 160 Mbps
- Utopia for ADSL (21 GPIO and 1 serdes)
  - 12.5% HRT, 22 MIPS for 8 Mbps
- 10/100 Ethernet MAC (MII)
  - 12.5% HRT, 26 MIPS for 200 Mbps
- UART, USB 1.1, GPSI, SPI, I2C, BlueRF (Serdes)
- PCMCIA, ISA (GPIO)
- IDE
PCI Software I/O Detail

- 25% peak MIPS allocated to Hard Real Time Thread
- Five instruction inner loop per PCI clock
  - Test IRDY, JMP, test FRAME, move data, JMP
  - One clock taken branch penalty
  - 24 chip clocks per PCI clock
  - 10.4 MHz PCI clock at 250 MHz
- Suspended thread wakes up on Request
  - Synchronize to PCI clock, assert Grant
- Parity disabled
- Meets PCI timing
IP3023 SOHO 802.11g Router

IP3023 Features:
• Proven Karlnet router features
• WPA
• Roadmap s/w support:
  • 11a / b / g Upper MAC
  • VPN termination
  • 11i/11e as it hits the market
  • Utopia for DSL integration

External Component BOM

<table>
<thead>
<tr>
<th>Qty</th>
<th>Part</th>
<th>ASP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>512kB</td>
<td>$1.30</td>
</tr>
<tr>
<td>1</td>
<td>IP3023-250</td>
<td>$12.00</td>
</tr>
<tr>
<td>3</td>
<td>10/100 Eth PHY</td>
<td>$2.40</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$15.70</td>
</tr>
</tbody>
</table>
# Example I/O Application Mapping

<table>
<thead>
<tr>
<th>I/O port</th>
<th>Hardware I/O</th>
<th>ADSL wireless Gateway</th>
<th>Home router</th>
<th>Super Wireless AP</th>
</tr>
</thead>
<tbody>
<tr>
<td>32 bits</td>
<td>Flash</td>
<td>Flash</td>
<td>Flash</td>
<td>Flash</td>
</tr>
<tr>
<td>8 bits</td>
<td>SDRAM</td>
<td>Utopia</td>
<td>WiFi</td>
<td>SDRAM+WiFi</td>
</tr>
<tr>
<td>16 bits</td>
<td>MII-1</td>
<td>Utopia</td>
<td>10/100 Ethernet</td>
<td>10/100 Ethernet</td>
</tr>
<tr>
<td>18 bits</td>
<td>MII-2</td>
<td>10/100 Ethernet</td>
<td>HomePlug</td>
<td>10/100 Ethernet</td>
</tr>
<tr>
<td>8 bits</td>
<td>Serdes/MII-3</td>
<td>USB</td>
<td>10BT to modem</td>
<td>BlueRF</td>
</tr>
<tr>
<td>8 bits</td>
<td>Serdes/MII-3</td>
<td>Telephone</td>
<td>USB</td>
<td>Lights</td>
</tr>
<tr>
<td>32 bits</td>
<td>GPIO</td>
<td>802.11g/PCI</td>
<td>Telephone</td>
<td>802.11g/PCI</td>
</tr>
<tr>
<td>16 bits</td>
<td>MII-4</td>
<td>802.11g/PCI</td>
<td>10/100 Ethernet</td>
<td>802.11g/PCI</td>
</tr>
</tbody>
</table>
BCM4710 + 2 SDRAM, 32 Mbit Flash

IP3023 + 4 Mbit Flash
Broadcom and IP3023

BCM4710 + 2 SDRAM, 32 Mbit Flash

IP3023 + 4 Mbit Flash
Broadcom and IP3023

BCM4710 + 2 SDRAM, 32 Mbit Flash

IP3023 + 4 Mbit Flash
Broadcom and IP3023, With Memory

BCM4710, 2 SDRAM, 32 Mbit Flash

IP3023, 4 Mbit Flash
## Summary

### New Instruction Set Architecture
- Deterministic multi-threading
- Software I/O – small, flexible
- Memory-to-memory
- Powerful bit manipulation

### Ubicom is driving the high-performance, low-cost, and small-size requirements of wireless networking

### IP3023 Chip
- 2nd Generation software I/O
- 8-way simultaneous multi-threading
- 250 MHz
- 320 KB on chip memory
- Highly flexible I/O