Single Chip CMOS Direction Conversion Transceivers for WWAN and WLAN

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Introduction

I. Market Requirements
II. Receiver Architectures
III. Sirific’s Virtual LO™
IV. Transmitter Architectures
V. Sirific’s Transceiver Platform and Implementation
VI. Conclusion
Cellular Market Forecasts

Wireless Market Forecasts by Standard

Source: Deutsche Bank (Jan 2004)

2008 Wireless Market Forecast by Standard

EDGE + WCDMA market will account for 62% of the overall worldwide wireless market

GSM, GPRS, EDGE and WCDMA combined will dominate the cellular market share
WLAN Market Forecasts

Worldwide WLAN Chipset Units

<table>
<thead>
<tr>
<th>Year</th>
<th>Units (in Million)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2001</td>
<td>10</td>
</tr>
<tr>
<td>2002</td>
<td>20</td>
</tr>
<tr>
<td>2003</td>
<td>30</td>
</tr>
<tr>
<td>2004</td>
<td>40</td>
</tr>
<tr>
<td>2005</td>
<td>50</td>
</tr>
<tr>
<td>2006</td>
<td>60</td>
</tr>
<tr>
<td>2007</td>
<td>70</td>
</tr>
</tbody>
</table>

Source: In-Stat/MDR 3/03

- Predominant increase in WLAN Hotspot locations as well as WLAN chipset units in the next few years
- Expected that 50% of units by 2006 will be multi-standard (802.11a/b/g)

- Cellular and WLAN market trends are driving for multi-standard, multi-band devices

I. Market Requirements

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VI. Conclusion
Until now, most receiver architectures have been limited either to narrow-band (GSM, GPRS, EDGE) or wide-band (WLAN, WCDMA), not both.
DC Offset Issues in Direct Conversion Radios

- DC offsets are common problem for direct conversion architectures and result from 5 physical effects:
  - RF leakage
  - LO-RF leakage
  - IIP2 (second order distortion) → Very bad for CMOS because of bad switching characteristics
  - Thermal DC offset
  - 1/f noise → Limiting factor for Direct Conversion CMOS

In order for IIP2 to be a “stable” measurement value, the following condition should hold:

(input referred second order harmonic) > (LO leakage level reference to the input)

<table>
<thead>
<tr>
<th>LO leakage = -99dBm</th>
<th>IM2 = -60 dBm</th>
<th>IIP2 “stable”</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO leakage = -66dBm</td>
<td>IM2 = -120 dBm</td>
<td>IIP2 “unstable”</td>
</tr>
</tbody>
</table>
1/f Noise in CMOS Circuits for Direct Conversion

- More important in CMOS
- Limiting factor for GSM/GPRS/EDGE direct conversion CMOS
- No “potential” fixes in CMOS
  - 1/f noise is more significant in CMOS technology
  - 1/f noise arises at baseband due to the switching of transistors in the mixers
  

LO Generation

- LO generation is the generation of signal(s) to down convert the RF signal without corrupting the data
- Some contributors of DC offset can be combated with LO generation

\[ l(t) \sin(\omega t) \rightarrow l(t) \sin(\omega t) \]

No external filters as in superhet radios

Has no energy at \( \omega \)
I. Market Requirements

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Virtual LO™ - Sirific’s Solution for LO Generation

* Sirific’s Virtual LO™ frequency planning technique eliminates the DC offset

\[
x(t) \rightarrow x(t) \times \phi_1(t) \times \phi_2(t) = x(t) \times \phi_{eff}(t)
\]

Has several conditions

\[
\phi_{eff}(t) = \phi_1(t) \times \phi_2(t)
\]
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Summary of Transmitter Architectures

- WLAN
- WCDMA
- EDGE
- GPRS
- GSM

Direct modulation is the only architecture that is not limited to any specific standard.
Transmitter Architectures – Direct Modulation

- **Advantages**
  - Simple architecture
  - Wide-band
  - Single LO

- **Disadvantages**
  - Limited gain control
  - Difficult to meet noise, linearity, carrier feedthrough, and quadrature accuracy (especially in GSM)

![Diagram of Transmitter Architectures – Direct Modulation]

Direct Modulation vs. Polar Loop

<table>
<thead>
<tr>
<th>Direct Modulation</th>
<th>Polar Loop</th>
</tr>
</thead>
<tbody>
<tr>
<td>+ supports other more complex modulations (i.e. WCDMA)</td>
<td>+ Lower noise (no TX filtering)</td>
</tr>
<tr>
<td>+ no calibration or complex loops</td>
<td>+ Add on to past GSM solutions (i.e. translational loop)</td>
</tr>
<tr>
<td>- Higher noise output (may require TX filtering switches – filters are about &lt;$0.20 in volume)</td>
<td>- supports only some modulations</td>
</tr>
<tr>
<td>- Requires Linear PA</td>
<td>- Requires calibration or complex loops that require power</td>
</tr>
<tr>
<td>- Carrier feed-thru/sideband requires consideration</td>
<td>- May require isolators (significant size and &gt;$1.00 in volume)</td>
</tr>
<tr>
<td>? Lower PA efficiency (higher power)</td>
<td>- May require PA controller chip</td>
</tr>
<tr>
<td></td>
<td>? Higher PA efficiency (lower power)</td>
</tr>
</tbody>
</table>
**Polar Loop vs. Direct Modulation System PAE for EDGE**

- **System PAE for a Polar Loop**
  - PA is limited by the LDO which is used for amplitude modulation
  - System PAE < 20% including LDO) at Pout = +28dBm for Polar Loop

- **No LDO is required for Direct Modulation**
  - System PAE ~ 25% at Pout = +28dBm for Direct Modulation

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**I. Market Requirements**

**II. Receiver Architectures**

**III. Sirific’s Virtual LO**

**IV. Transmitter Architectures**

**V. Sirific’s Transceiver Platform and Implementation**

**VI. Conclusion**
Dynamic Spurious Control (DSC) is used to boost radio performance in the presence of a large out-of-band blocker within a packet (i.e. for GSM)

- The interferer is sensed within the high frequency path and I/Q path.
- With these two pieces of data $\phi_2$ is modified which automatically modifies $\phi_1$. 
Rx total chain measurements

<table>
<thead>
<tr>
<th>Receiver</th>
<th>850/900</th>
<th>1800/1900</th>
<th>WLAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise Figure</td>
<td>2.8dB</td>
<td>3.0dB</td>
<td>3.5dB</td>
</tr>
<tr>
<td>LO Re-radiation</td>
<td>-133dBm</td>
<td>-103dBm</td>
<td>-108dBm</td>
</tr>
<tr>
<td>IQ Phase Error</td>
<td>&lt; 1°</td>
<td>&lt; 1°</td>
<td>&lt; 1°</td>
</tr>
<tr>
<td>IQ Amplitude Error</td>
<td>&lt; 0.5dB</td>
<td>&lt; 0.5dB</td>
<td>&lt; 0.5dB</td>
</tr>
<tr>
<td>Maximum Gain Range</td>
<td>95dB</td>
<td>95dB</td>
<td>80dB</td>
</tr>
<tr>
<td>IIP2 (min)</td>
<td>45dBm</td>
<td>54dBm</td>
<td>66dBm</td>
</tr>
<tr>
<td>ΔNF with -26dBm</td>
<td>4dB</td>
<td>4dB</td>
<td>-</td>
</tr>
<tr>
<td>Blocker @ 3MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LNA Power</td>
<td>18mW</td>
<td>18mW</td>
<td>18mW</td>
</tr>
<tr>
<td>Mixer Power</td>
<td>41mW</td>
<td>41mW</td>
<td>41mW</td>
</tr>
</tbody>
</table>

Gm-C Baseband Filter, VGA and DCOC

Fast and slow DCOC

Filter Tuning Control
Gm-C Capacitor Assignments

Gm-C Baseband Filter, VGA and DCOC

<table>
<thead>
<tr>
<th>Baseband Filter</th>
<th>850/900</th>
<th>1800/1900</th>
<th>WLAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>3dB Bandwidth</td>
<td>204kHz</td>
<td>204kHz</td>
<td>7.3MHz</td>
</tr>
<tr>
<td>Rejection</td>
<td>64dB @ 600kHz</td>
<td>64dB @ 600kHz</td>
<td>62dB @ 25MHz</td>
</tr>
<tr>
<td>Baseband Filter Power (Max Gain)</td>
<td>20mW</td>
<td>20mW</td>
<td>54mW</td>
</tr>
</tbody>
</table>
Tx Chain Measurements

<table>
<thead>
<tr>
<th></th>
<th>850/900</th>
<th>1800/1900</th>
<th>WLAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Carrier Suppression</td>
<td>&gt;40dB</td>
<td>&gt;40dB</td>
<td>&gt;40dB</td>
</tr>
<tr>
<td>Sideband Suppression</td>
<td>38dB</td>
<td>38dB</td>
<td>&gt;35dB</td>
</tr>
<tr>
<td>PN@20MHz@max P</td>
<td>-154dBc/Hz</td>
<td>-149dBc/Hz</td>
<td>-</td>
</tr>
<tr>
<td>Gain Range</td>
<td>41dB</td>
<td>41dB</td>
<td>40dB</td>
</tr>
<tr>
<td>Max output power</td>
<td>8dBm</td>
<td>8dBm</td>
<td>4dBm</td>
</tr>
<tr>
<td>Mixer Power</td>
<td>34mW</td>
<td>34mW</td>
<td>65mW</td>
</tr>
<tr>
<td>PPA Power</td>
<td>77mW</td>
<td>77mW</td>
<td>65mW</td>
</tr>
</tbody>
</table>

EDGE Output spectrum from Tx

- EDGE modulation
- Pout = 0dBm
- Passes EDGE mask
RF Synthesizer

Serial Interface

4bit fast acquisition

PFD

f_ref/M

f_vco/N

CP

ΣΔ

Fast acquisition

+2/+4

RF Input

To Analog Baseband

Synthesizer Measured Performance

<table>
<thead>
<tr>
<th>Synthesizer</th>
<th>GSM</th>
<th>WLAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO Frequency Range</td>
<td>3.4GHz to 3.9GHz</td>
<td>4.5GHz to 5.0GHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>200kHz</td>
<td>200kHz or 1MHz</td>
</tr>
<tr>
<td>Settling Time (to 100ppm)</td>
<td>185µs</td>
<td>-</td>
</tr>
<tr>
<td>Phase Noise (at mixer port)</td>
<td>-90dBc/Hz @ 10kHz</td>
<td>-85dBc/Hz @ 100kHz</td>
</tr>
<tr>
<td></td>
<td>-140dBc/Hz @ 3MHz</td>
<td>-131dBc/Hz @ 3MHz</td>
</tr>
<tr>
<td>CP, Dividers, Loop Filter Power</td>
<td>36mW</td>
<td>36mW</td>
</tr>
<tr>
<td>VCO Power</td>
<td>11mW</td>
<td>11mW</td>
</tr>
</tbody>
</table>
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Summary

- Multi-band, Multi-standard applications are a market requirement
  - Network operators and handset OEM/ODMs require low-cost high performance multi-mode solutions

- The consumer demand for wireless data services is driving the EDGE, WCDMA and WLAN markets

- CMOS solutions provide high integration and low cost
  - Applying CMOS to narrow-band cellular standards presents many design challenges

- Direct Conversion is the receiver architecture of choice for multi-standard applications
  - Eliminating DC Offset is critical

- Direct Modulation is the transmitter architecture of choice for multi-standard applications
  - Reducing Carrier Feedthrough and improving Quadrature Accuracy

- Sirific’s Virtual LO™ and Dynamic Spurious Control are methods used to design a multi-band, multi-band direct conversion CMOS transceiver