SolarFlare Communications

- Headquarters: Irvine, CA
- Product Focus: 10Gbps UTP Ethernet chip set
- Fabless business model with foundry CMOS process
- Key IP: DSP algorithm deriving its roots from NASA deep space communications
- Technology first demonstrated in March 2004
Why UTP?
It’s not *just* about running on installed cable

<table>
<thead>
<tr>
<th>Optical Fiber and Modules</th>
<th>UTP and 10GBASE-T PHYs</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Terminations are very expensive and require skilled labor to install</td>
<td>• RJ45 is cheap, plastic, installed in field by any IT manager</td>
</tr>
<tr>
<td>• Optical modules necessarily involve the mechanical assembly of many technologies: VCSELs, PIN diodes, laser drivers, transimpedance amps and SerDes chips.</td>
<td>• UTP PHYs are implemented in vanilla CMOS and are on a roadmap to single chip integration – lower COGs by construction</td>
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<tr>
<td>• Optical modules are, by construction, one per port</td>
<td>• UTP PHYs are capable of multi-port-on-a-chip implementations as lithography progresses – dramatically lowering price per port</td>
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<tr>
<td>• Optical modules are designed to operate at only one data rate and only purchased in applications where that data rate is needed</td>
<td>• UTP PHYs are rate adaptive – making them attractive for PC LOM adoption where they are sold as “future proofing”</td>
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</table>
What’s wrong with CX-4?

- Short reach
  - Standardized to 15m; Some solutions up to 30m
  - The problem: Sweet Spot of Data Center applications is between 40m and 70m
    - Because of patch panel connections

- Expensive Cabling
  - $200 for 15m link with connectors
    (compare to $15 for same link on Cat6)

- Thick cumbersome cable and large connectors

- Can not be terminated in the field

Source: computercablestore.com

Technology Behind Ethernet Evolution

- Transitions require new technology allowing to emerge

- Near-End Crosstalk
- Far-End Crosstalk

- Inter-Symbol Interference

- Conventional Wisdom Channel Capacity

- New model Channel Capacity

- 10GBASE-T

- 1000BASE-T

- 10BASE-T

- Analog Linear

- Perceived Channel Capacity
Why is 10G on UTP so difficult?

- Very small receive signals swamped by ...
- Many sources of noise:
  - Far-End Echo
  - Near-End Crosstalk (NEXT)
  - Far-End Crosstalk (FEXT)
  - Inter-symbol interference (ISI)
  - Electromagnetic Interference (EMI)

Design Philosophy

- Evolutionary build on 1000BASE-T
  - Revolutionary complexity/performance enhancers
- Need to enhance treatment of media impairments
  - NEXT mitigation (less noise)
  - FEXT mitigation (less noise)
  - EMI friendly/Spectral efficiency (more bits/baud)
- Best complexity / performance tradeoff while being Standards compatible
### Comparison w/ 1000BASE-T

<table>
<thead>
<tr>
<th>1000-BASE-T</th>
<th>10GbE Solution [UTP]</th>
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<tbody>
<tr>
<td>Multilevel coded PAM signaling (2-bits/symbol)</td>
<td>Multilevel coded PAM signaling (3-bits/symbol)</td>
</tr>
<tr>
<td>5-level with trellis code across pairs</td>
<td>10-level with trellis code across pairs</td>
</tr>
<tr>
<td>Full duplex echo-cancelled transmission</td>
<td>Full duplex echo-cancelled transmission</td>
</tr>
<tr>
<td>125 Mbaud, ~80 MHz used bandwidth</td>
<td>833 Mbaud, ~400 MHz used bandwidth</td>
</tr>
<tr>
<td>Moderate NEXT cancellation</td>
<td>High-Performance NEXT cancellation</td>
</tr>
<tr>
<td>No specified FEXT cancellation</td>
<td>High-Performance FEXT cancellation</td>
</tr>
</tbody>
</table>

### Measured Radiated Emissions

![Graph showing measured radiated emissions for different scenarios.](image)

- 100 meter channel
- 50 meter span Cat 5e
- FCC Class A limit
### SolarFlare IP Platform

<table>
<thead>
<tr>
<th>Key Intellectual Property</th>
<th>Solarflare Uniqueness</th>
<th>Impact on Design</th>
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<tbody>
<tr>
<td>Multilevel Coded Modulation</td>
<td>Better bandwidth utilization</td>
<td>Enhanced tolerance to cable variability</td>
</tr>
<tr>
<td>Adaptive Line Equalization</td>
<td>Much higher performance</td>
<td>Mitigates ISI</td>
</tr>
<tr>
<td>New Echo and NEXT mitigation architecture</td>
<td>7x circuit area reduction for function</td>
<td>Fabrication feasibility</td>
</tr>
<tr>
<td>Combined FEXT and equalization circuits</td>
<td>6x circuit area reduction for function</td>
<td>Economic circuit realization</td>
</tr>
<tr>
<td>Interwoven A/D and DSP architecture</td>
<td>Digital implementation of traditionally analog circuit attributes</td>
<td>Enable utilization of CMOS A/D</td>
</tr>
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</table>

#### Chipset Details

**DSP:**
- 0.13μ CMOS
- 25 x 25 mm 575 pin BGA package
- 5.4 million gates + 2 Mbits memory

**AFE:**
- 0.18μ CMOS
- 23 x 23 mm 473 pin BGA package
- 2.76 million transistors (0.7 million eq. Gates)
AFE Highlights

- Integrates:
  - Four 10-bit, 1Gsps analog-to-digital converters
  - Programmable gain amplifiers
  - PLL clock multiplication and distribution circuits
- 0.18μ CMOS technology
  - Low risk, low cost
- 2.7 Million Transistors

AFE Block Diagram
AFE Die Layout

Key Challenges and Mitigation Strategies

- High input bandwidth (500MHz) needs
  - Custom sampling circuit with very short sampling aperture and high bandwidth PGA front end.
- Low jitter and low skew clock distribution
  - Self adjusting PLL based closed-loop architecture
- Low front-end noise and high linearity requirements
  - Careful partitioning of gain elements in signal path
- Channel to channel noise coupling
  - Dedicated power and ground systems per channel
  - Isolation guard rings and on-chip shielding structures
  - Extensive packaging/substrate modeling
  - Flip-chip packaging for bond-wire inductance elimination