A Fast Powertrain Microcontroller

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Never stop thinking.

Trend: Global Chassis Control: Functions within Vehicle Dynamic & Powertrain Grow Together
**Trends:**

- Distributed systems in vehicles
  - Distributed smart sensors, actuators, computation
  - New opportunities for scalability, flexibility, reusability, composability
  - Infineon is member of the FlexRay consortium

- Software will play an increasing role
  - Vehicle’s “Drive & Feel” will become increasingly defined by algorithms and software
    - i.e. SW will become a significant element in brand differentiation
  - Software complexity increases and will be a compilation of different vendor’s contributions
    - A change in SW development methodology will occur
    - New SW interfaces will become standard, encapsulation will be needed
  - Infineon is member of the AutoSAR development partnership

**Powertrain Management**

**Chassis Management**

**Energy Management**

**Vehicle Guidance**

**Powertrain Trends**

- Cam-less Engine
- Electronic Turbo Charger
- Direct Injection
- Indirect Injection
- Full-Hybrid Vehicle
- Fuel Cell Vehicle
- Hybrid Vehicle
- Electric Vehicle
- Mini-Hybrid Vehicle
- Low Emission & Low Consumption Vehicle
Less Fuel Consumption and Cleaner Engines - Driving Forces for Higher Performance

Average Fuel consumption  
AUDO-NG
  32Bit
  2002: AUDO
  16Bit
  1992: C167
  1990: 80C166
  1987: 80535 EURO1
  1978: 8048

Year of introduction : Infineon Microcontroller Type
EUROx=European Emission Standards

Optimized Partitioning for Powertrain

Today - Example Conventional Engine Management

Tomorrow Optimized Chip Set by Infineon

=> Saves System Costs
AUDO-Next Generation (NG): TC1796 -
At a Glance

- 32-bit superscalar TriCore® V1.3 CPU
- 32-bit Peripheral Control Processor (PCP2)
- Multi-channel DMA controller
- Powerful & flexible peripheral set
  - 2.5 x GPTA® (flexible timer array)
  - MultiCAN (4 nodes)
  - 2x ASC and 2x SSC Interfaces
  - 2x µS-Bus Interfaces (MSC)
  - Multi-Processor Interface (MLI)
  - Multi-channel ADCs, FAST ADC
- On-chip Memory:
  - 2.1 MByte Flash Memory (partially supports EEPROM emulation)
  - 192 kByte SRAM, 16 kByte Program Cache
  - 48 kByte SRAM for PCP2
- Digital Port Supply Voltage 2.3V - 3.3V
- Full automotive temperature range
- Package: P-BGA 416

AUDO-NG: TC1796 -
The Three Layer Implementation

To allow the right function partitioning with clear interfaces, Infineon has design the three layer approach.
Tricore can execute up to 3 instructions in parallel per cycle.

In parallel, the PCP executes its own instructions.
Data Level Parallelism

- TriCore’s packed arithmetic allows to process up to 4 data per instruction
- In parallel, the PCP processes e.g. data from the GPTA
- The DMA unit transfers data e.g. from the FADC
- Intelligent peripherals handle data in parallel

Non-Intrusive Data Transfer Capability
No Penalty for TriCore and PCP

Cost for the TriCore/PCP
- Usage = 0
- Wait = 0

- 16 bit 10 Mbit/s
- 16 bit 10 Mbit/s
- > 500 k.Samples/s
- > 500 k.Samples/s
- 3.5 M.Samples/s

ADC
ADC
FADC
MLI
DMA
SSC
SSC
DPRAM
Remote Peripheral Bus
64
64
>30 Mbit/s
TriCore Architecture
Designed for Embedded Real Time Applications

- High performance 32-bit core
  - The first unified RISC/DSP architecture
  - 150 MHz / 4 stage superscalar pipeline
- Fast context switch mechanism
- Fast, deterministic interrupt mechanism
- Floating point unit (optional)
- Flexible coprocessor interface
  - For up to 3 coprocessors
- Optional memory management unit *
- Configurable cache and memory sizes
- Fast local memory bus system

* not implemented in TC1796

Features
- Up to 4 x 255 request nodes (SRN), concurrently supported
- Parallel arbiter HW to select highest interrupt & clear when accepted
- Automatic context save during branch to interrupt routine

Benefits
- Meets real-time requirements
- Zero software overhead
- Ease of programming, High flexibility
- Large number of SRNs
- Flexible grouping of request into priority groups

Arbitration
Peripheral 1  Peripheral 2  Peripheral 3  Peripheral 4
SRN  SRN  SRN  SRN

FPI Bus

Interrupt Control Unit (ICU)
PCP2 – Peripheral Coprocessor

- PCP2 is a full 32 bit user programmable processor dedicated to communication and driver activities
- Off-loads TriCore from handling interrupt tasks (hardware arbitration & register context switch, 255 priority levels)
- Includes DMA engine
- PCP2 can run autonomously Flywheel, Injection, Ignition… driver software

Modules: GPTA – General Purpose Timer Array
Unified High Functionality and Flexibility

- Function blocks for
  - Input signal conditioning
  - and analysis
  - Digital PLL
  - Capture/Compare Cell Arrays
- Flexible timer array

- Highly functional structure:
  - Largely autonomous operation requiring low or no SW overhead
  - Main CPU not loaded with highly repetitive tasks
- Permits optimized use of timer cells
  - Scalable functionality avoids functional overhead
  - Maximizes system functionality

Architecture driven by needs for:
- 8-cylinder combustion engines
- 3-phase AC-motor
**Modules: MultiCAN**

Feature Set and Module

- CAN functionality conform to CAN specification V2.0 B active (compliant to ISO 11898)
- 4 independent CAN nodes available
- 128 independent message objects (message objects are shared by the CAN nodes)
- Data transfer rate up to 1M baud, individual programmable for each node
- Flexible and powerful message transfer control and error handling capabilities to offload CPU
- Automatic gateway mode support
- 16 individually programmable interrupt outputs
- CAN Analyzer Mode for bus monitoring
- Time-Triggered CAN (TTCAN) support

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**Modules: Fast ADC**

Application Example: Knock Detection

- Remove expensive external filters
  - Reduce system cost
- Allow better utilization of the input signal range
- Allow better signal diagnosis
  - Self test, explore signal consistency
- High sampling frequency
  - Up to 3.5 M sample/s with 10 bit resolution
- Configurable HW differential amplifier
  - Reduce cost on external HW
  - Improved common mode noise rejection
- Configurable digital data compression
  - Reduce software load
**Modules: MLI / MSC**

Multicore/Device Link via High Speed MLI and MSC

- Micro Link Interface (MLI) to connect smart companion devices
- Micro Second Channel (MSC) to primarily connect power devices
- Benefit: Highly configurable and scalable
- \( \downarrow \) the wiring on the board
- \( \downarrow \) amount of pins per package
- \( \uparrow \) the bandwidth but \( \uparrow \) EMI
  - Low swing and smooth edge
- Open license policy on MLI, MSC
  - IFX will provide “Open Market Specification”

**Tuning Protection and Authentication**

- IP Snatcher
- Vehicle Theft
- Flash EEPROM
- CPU
- Debug
- RAM
- EEPROM
- TTCAN
- anti theft system
**TC1796ED**  
Emulation Device

- TC1796ED covers complete emulator functionality, fast prototyping and calibration
- Emulation logic is next to production chip
  - On the same silicon
- High frequency capability
- High amount of traceable signals (on mask level)
- Production & emulation have the same behavior
- Easy link to standard PC e.g. USB
- TC1796 and 1796ED using the same footprint
  - No need to develop different PCB
  - Extra balls for the ED
- Tool connector on top

**Infineon’s approach - high functionality and cost effective Interface with TC1796ED**

**Traditional approach - expensive solution due to additional necessary HW**

- Serial link, e.g. Ethernet, USB
- Thick, Short Nexus Cable
- Emulator HW
- Calibration HW

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**TC1796 and TC1796ED**

- Mass Production Device: Bonding
- Emulation Device: Bonding with EEC
Summary

- TC1796 serves upcoming trends in powertrain applications
  - Fullfills highest performance requirements including soft- and hard real-time
  - Intelligent peripherals
  - Optimized bus system
  - Unified CPU/DSP and peripheral coprocessor
  - Reduces system cost
  - Powerful emulation support

http://www.infineon.com/

Thank you for your attention

Questions?

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