A 90nm embedded DRAM single chip LSI with a 3D graphics, H.264 codec engine, and a reconfigurable processor

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outline
- What is PlayStation® Portable (PSP™)
- PSP™ system chip block diagram
- 3D-graphics module
- H.264( AVC) Decoder
- Reconfigurable processor
- Embedded DRAM
- Chip implementation
- Conclusion
What is PlayStation® Portable (PSP™) New Handheld Video Game System

- 3D-CG Games with High Quality Video/ Sound
- 4.3 inch, Wide Screen (16:9) TFT LCD
- UMD™, High-Capacity (1.8GB) Optical Disc
- ATRAC3 plus, AAC, MP3 for Music
- AVC/ @MP for Picture/ Movie
- Li-ion Battery

PSP™ System Chip Block Diagram
Game/ Media processing unit

- Game processing unit
  - CPU Core
    - MIPS R4000 32bit Core: 1-333MHz
    - FPU, VFPU (Vector Unit)
  - 3D graphics
    - ‘Rendering Engine’ + ‘Surface Engine’
    - 2MByte eDRAM (VRAM): 512bit/ 166MHz bus I/F

- Media processing unit
  - Media Engine
    - MIPS R4000 32bit Core with FPU
    - 1-333MHz
  - H.264 codec engine
  - H.264 hardware accelerator
  - VME (Virtual Mobile Engine)
    - A reconfigurable processor to decode audio/video codec

eDRAM & I/O

- eDRAM
  - Total capacity of 4Mbytes
  - One half for the game processing unit
  - The other half for the media processing unit

- I/O
  - Mobile DDR I/F
  - USB 2.0 (Device)
  - Memory Stick™
3D-Graphics Module
Surface Engine Specification

Surface Technology
• High-speed tessellation logic of Bezier and Spline Surfaces.
• Hardware Transformation and Lighting.

Geometry Blending
• (up to 8 matrices) for skinning.

Vertex Blending
• (up to 8 vertices) for morphing.

Surface Technology
These two models have the same data size

Surface model
Polygon model
**Geometry Blending (Skinning)**

Relaxed Pose

Skinning OFF

Skinning ON

**Vertex Blending (Morphing)**

Key Frame 1

Key Frame 2
Rendering Engine Specification

Drawable Primitives
- supports Point, Line, Triangle, Rectangle, Bezier and Spline.

Graphics Functions
- Directional/Point/Spot Lighting
- Clipping
- Environment Mapping
- Projection Mapping
- Texture Mapping
- Fogging
- Alpha Blending
- Depth Test
- Stencil Test
- Dithering
- 16/32 bit pixel color

Frequency & Performance

Frequency
- Frequency: 166 MHz
- Graphics Memory: 2 Mbytes

Performance (@166MHz)
- Surface Tessellation (divide by 16x16): 58 K Patches/sec
- Geometry: 35 M Polygons/sec
- Rendering Setup: 35 M Polygons/sec
- Pixel Fill Rate: 664 M Pixels/sec
H.264 (AVC) Decoder

Features

- H.264 | ISO/IEC 14496-10 (MPEG-4 Part10) Decoder
- Supports Main Profile
- Supports Up to Level3 (720x480@30fps)
H.264 Decoder Block Diagram

Reconfigurable Processor
(Virtual Mobile Engine™)
Virtual Mobile Engine™ (VME) Concept

VME is “virtual dedicated accelerator” using Dynamic Reconfigurable Architecture for Low-power and Programmability

VME Structure

- Works as Dynamic Reconfigurable vector engine
- Reconfigured on the fly
- One cycle context switch
- Coarse grain heterogeneous type
- Native 24bit data-width
- Max Clock Freq. 166MHz
**Typical VME Operation**

1. **CPU**
2. **memory**
3. **Bus I/F**
4. **DMAC**
5. **Ctl Reg.**
6. **Context Reg.**
7. **Add. Gen.**
8. **Local Memory**
9. **Reconfigurable Datapath**

**Virtual Mobile Engine™ (VME)**

(1) **set**
(2) **load**
(3) **execute**
(4) **int. or pol.**
(5) **store back or reuse LM data in next exe.**

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**VME Applications**

*Only existing low-power Dynamic Reconfigurable Engine used for Consumer Product*

*World's First Consumer Product using Reconfigurable architecture!*

- PSP™
  - game sound
  - audio codec
  - sound effect
  - video codec

- Network Walkman (HDD)
- CD Walkman
- MD Walkman

Audio ATRAC3 Dec
4mW @1.2V,0.18um

Feb. '03 '04
Embedded DRAM

Specification

- **Configuration**
  - [1024row x 32col x 128bits x 2Bank] x 4Macro

- **AC Spec**
  - tCK(min.): 6ns < 166MHz>
  - tRC(min): 30ns
  - CAS latency: 2clk

- **Special Function**
  - 1Cycle Read-Modify-Write operation for 3D graphics

PSP™ 1MB eDRAM (128bit 2Bank)
eDRAM Macro Configuration

Read modify write
- 128bit Read + 128bit Write
- Data can be read and written at the same time in generating 3D graphics
- Normal read/write mode is also available

RMW Timing Chart

< Read modify write Like GRAPHICS SYNTHESIZER of PS2>
- 8 state write address FIFO
- 2 Bank interleave operation
Chip implementation

Low power control

- Core voltage control
  - VDD = 0.8 - 1.2V
- Clock frequency control
  - 1-333MHz: CPU clock
  - 0.5-166MHz: Bus clock
- Clock ON/OFF control
  - Clock supply is gated at clock control unit.
  - CPU can control clock supply to each block
- Independent power ON/OFF control
  - 3D-Graphics unit
  - H.264 unit
  - reconfigurable engine (VME)
### Physical chip implementation

#### Specifications

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### Conclusion

- A 90nm embedded DRAM single chip LSI for PSP™ has been developed.
- It has
  - 3D-graphics module
    - with Rendering Engine + Surface Engine
  - H.264(AVC) H.W. Decoder
  - Reconfigurable processor (VME)
  - 4Mbyte eDRAM
- This chip will be manufactured by Sony Semiconductor Kyushu Corporation at NAGASAKI, Japan.