Super Companion Chip with Audio Visual Interface for Cell Processor

Takayuki Mihara 1, Hiroki Muroga 1, Hiroshi Doi 1, Tadashi Yabuta 1, Yoichiro Iwagami 1, Kenichi Ishii 1, Naohiko Okamoto 1, Kazuki Iwata 1, Yoshimasa Aoyama 1, Takeshi Takamiya 1, Naoki Sugawa 2

1. Toshiba Corporation
2. Toshiba Microelectronics Corporation
Outline

- Background
- What is Super Companion Chip (SCC)?
- Processing Flow
- SCC Architecture
- Technology and Chip Implementation
- Conclusion
Motivation

- To provide software based digital consumer solution for Cell processor such as Digital TV, Audio Visual Server, etc.

- To establish GHz high bandwidth connection between Cell and ultra high speed peripherals on Super Companion Chip (SCC).
Requirements from Market
- Multi Tasks Processing Simultaneously -

Key Feature:
Real Time Audio Video Processing

- Multi Recording
- Time Shift Play
- Multi Screen

Satellite
SDTV
Terrestrial
HDTV
CATV
Streaming
Internet
Web, Streaming
Storage
HDD
HD-DVD
PC Monitor
DTV
Home Network
Cell Processor Overview

- Power Processor Element (PPE)
- Synergistic Processor Element (SPE)
- Dual XDR DRAM channels
- Flexible I/O Interface
- Element Interconnect Bus
Features of Cell Processor

- **Resource Management Capability**
  - Reserve Memory & I/O Bandwidth for up to four tasks.

- **Isolation Facility**
  - Each SPE is isolatable from outside for flexible secure programming.

- **Multi OS Support**
  - Run multiple OSs simultaneously.
  - e.g. Linux + Real-time OS
Features of SCC

- **For Real Time Processing**
  SCC internal bus has the bandwidth reservation capability for the each resources.
  - TDM arbitration

- **For Tight Security**
  The HW random number generator and several kinds of HW Encryption/Decryption functions are implemented.

- **For Multi OS Support**
  Every bus master module have the address space restriction mechanism.
  To prevent the IO resource conflict between OSs.
Outline

- Background
- What is Super Companion Chip (SCC)?
- Processing Flow
- SCC Architecture
- Technology and Chip Implementation
- Conclusion
SCC I/O Category

For versatile A/V system
- DDR2 DRAM I/F for Video RAM.
- Video output / Audio output.
- Video input / Audio input.
- Digital AV equipment connection I/F (IEEE1394).
- Digital tuner I/F (TS I/F).

For computer system
- Standard PC I/F (PCI-Express, PCI, USB2.0).
- High-speed Network I/F (Giga Bit Ethernet).
- Storage device I/F (Parallel ATA).
Outline

- Background
- What is Super Companion Chip (SCC)?
- Processing Flow
- SCC Architecture
- Technology and Chip Implementation
- Conclusion
Audio/Visual Processing Steps

< Digital Broadcasting >

1. TS Input → Multi2 Descramble → Demux
2. Scramble → HDD
3. Descramble
4. Character
5. Video Dec → I/P → Scaling → α Correction → NTSC En or HDMI
6. Audio Dec → DAC → Audio Output
7. Video Output

From BS Digital Tuner

< Digital Broadcasting >
Audio/Visual data flow

Taking digital broadcasting and Outputting A/V data with time shift function.

1. TS I/F → FlexIO → Cell ↔ XDR → FlexIO

2.

3. ATA I/F → FlexIO → Cell ↔ XDR → FlexIO

4.抜

5.

6. DMAC → DDR2 → Video Output

7. Audio Output

(SCC from/to Cell)

(Data Transfer in SCC)
Data Processing Flow

1. Transferring the data from TS I/F to Cell Processor.
2. Processing the data with XDR.
3. Recording the data on HDD.
4. Reading the data on HDD.
5. Processing the data with XDR.
6. Transferring the data from XDR to DDR2, Audio I/F.
7. Transferring the data from DDR2 to Video out I/F.
Outline

- Background
- What is Super Companion Chip (SCC)?
- Processing Flow
- SCC Architecture
- Technology and Chip Implementation
- Conclusion
Key Architecture (1/2)

- Internal Bus Architecture
  - Quality of Service (QoS)
    - Bandwidth allocation by bus arbitration mechanism (with priority in every cycle. TDM.)
  - Hierarchical Architecture
    - Dividing the bus according to the required features.
      - Real time bus and Best effort.

- DDR2 memory interface
  - Dedicated DMA controller
    - For streaming data.
Other Features

- Virtual Channel Mechanism
  To avoid blocking for data flow.

- Multiple thread mechanism
  Multi/Single threads are alternative.

- Pipelined data processing

- Data ordering mechanism
**FlexIO controller**

- Virtual Channel/Thread correspond to Cell functionality
  - Master Path: 8
  - Slave Path: 4
- Priority Control
Dedicated DMA controller

< For DDR2 memory >

- High bandwidth
  XDR $\rightarrow$ DDR2
  DDR2 $\rightarrow$ XDR
- 4 Virtual Channel(thread)
- Multi/Single threads
The each maximum bus bandwidth (2.66 GByte/s) is sufficient for the every required module bandwidth.
The bandwidth allocation mechanism can satisfy the BUS requirement from each module/bus bridge.
Outline

- Background
- What is Super Companion Chip (SCC)?
- Processing Flow
- SCC Architecture
- Technology and Chip Implementation
- Conclusion
- **Process**
  - 90nm CMOS Process
  - 7 Layer Cu

- **Frequency**
  - 333MHz

- **Package**
  - PBGA[FC], 1385pin, 40mm², 1mm pitch

- **Chip Size**
  - 12.71mm x 12.71mm

- **VDD**
  - Core: 1.2V
  - I/O: Multiple voltages for various peripherals
Outline

- Background
- What is Super Companion Chip (SCC)?
- Processing Flow
- SCC Architecture
- Technology and Chip Implementation
- Conclusion
Conclusion

- Super Companion Chip for “Cell” processor system has been successfully developed.

- Both rich audio visual features supporting HD and PC I/O features are integrated on the chip.

- Simultaneous 48 MPEG-2 SD stream decoding has been demonstrated by utilizing SCC’s high bandwidth bus with QoS capability.