A 1-GHz Configurable Processor Core  
— MeP-h1 —

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Outline

- Background
- Pipeline Structure
- Bus Interface
- Implementation
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Configurable Processor

- Customize a processor during RTL design
- Configurations
  - Cache config., Local RAM config., bus width, etc.
- Extensions
  - User customized instructions (DSP instruction extension)
  - Self-running hardware blocks (Hardware engines)

A simple controller
MeP-h1 Design Trade-off

High performance & high frequency
- Target: 1GHz@65nm

Configurable Processor
- Fully synthesizable
- ASIC standard design flow
  - 1-port synchronous SRAM
- A simple controller for extensions

Pipeline Design Issues
- Branch latency
- Local memory latency
- Extension i/f latency
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Pipeline Structure

9 stages for load inst.

Processor core

Fetch & Decode

Branch predecode

I(Integer)-Pipe
M(Memory)-Pipe
A(Auxiliary)-Pipe
V(Variable)-Pipe

DSP inst. extension

HW engine extension
Instruction Fetch Unit

- Branch predecode & prefetch
  - No branch prediction mechanism
Branch Prefetch

- Branch penalty
  - Branch taken: 1 – 4 cycles (cf. 4 cycles w/o branch prefetch)
  - Branch not-taken: 0 cycles
- Repeat (loop) inst. iteration penalty: 0 cycles
Average branch penalty: 1.8 cycles

More than 80% of branch penalty is less than or equal 2 cycles
Load Data Forwarding

MeP-c3
- 5-stage pipeline

Load penalty = 1 cycle

MeP-h1

Clock adjustment

Load penalty = 2 cycles
Extension I/F Latency

- **MeP-c3**
  - ex. 350-400MHz@90nm
- **MeP-h1**
  - ex. 1GHz@65nm

→ Tightly coupled extensions

→ Loosely coupled extensions
Tightly / Loosely Coupled Pipelines

- DC
- GPRs
- ROB
- I-Pipe
- M-Pipe
- A-Pipe
- V-Pipe
- LA
- LD
- M1
- M2
- SB
- E1
- E2
- RB
- Bypass 1
- Bypass 2
- Processor core
- DSP inst. extension
- HW engine extension
- VD
- VE
- V1
- III
- Vn
- VC
- An
- AC
- A1
- A2
- A3
- III

Tightly coupled
Loosely coupled

Dashed line for loosely coupled component.
Structure of ROB and GPR

- **ROB** (Reorder buffer)
  - 8 entries
  - 4 write ports
  - 3 read ports

- **GPRs**
  - 32 bits x 16 words
  - 1 write port
  - 2 read ports
DSP Extension Interface

Processor Core

V-Pipe

• dsp Rn,Rm,code
Rn = func(Rn, Rm, code)

DSP inst. extension

add   $8,4
lw    $7,($8)
add    $8,4

dsp0 $0,$1
dsp0 $2,$3
dsp0 $4,$5

Command
DC | VD | VE | V1 | V2 | V3 | VC | WB

M2   SB  ROB
M1   LA  LD  ROB
E2   E1  ROB
RB   ROB

Completion
Commit
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SoC Architecture

- **MeP module**: MeP-h1 processor core, DMAC, Extensions
- **Global bus**: Based on OCP2.0
- **Local Bus**: MeP module
- **Host CPU bus**: Host CPU ex. ARM
- **Peripheral bus**: Peripherals
- **Bus bridge**: Debug module, MeP module
- **Control bus**: MeP module
- **Extensions**: MeP module
- **JTAG**: Debug module
- **PC trace**: Debug module, MeP module
- **Run control unit**: Debug module
- **Memory Controller**: SDRAM
- **SDRAM**: Memory Controller

**HW module**

**Host CPU**: ex. ARM
Bus Interface

- Based on OCP* 2.0
  - Split bus transaction
  - Single request burst
  - Posted write
  - Pipelined request and response
    - 2 outstanding requests
  - Master bus reset and slave bus reset

*) OCP: Open Core Protocol
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Configurations

- **I$: 8KB, direct-mapped**
- **I-RAM: 4KB**
- **D$: 8KB, direct-mapped**
- **D-RAM: 4KB**
- **Bus width: 64 bits**
- **Debug function:**
  - Hardware breakpoints,
  - Single step
  - PC trace (8KB trace memory), etc.

Extensions

- **DSP instruction extension**
- **4 hardware engines**
First Implementation

- Toshiba 65nm CMOS process
- Size: 1.58 mm x 2.96 mm
- Gate counts: 250K gates (core only)
- Power consumption*
  about 1W @ 1GHz, w/o clock gating
  *) estimated by total of Tr. sizes and wire loads.
- Static Timing Analysis result
  Clock margin = 80 ps
  Critical path delay = 918 ps
  Total = 998 ps → 1GHz
Lab. Result

Voltage vs. Frequency (Room temp.)

Supply Voltage [V]

Frequency [MHz]
Conclusion

- Configurable processor aims to high performance & high operating frequency

- Pipeline design
  - Deeper pipeline stages
  - Branch predecode and prefetch
  - Relaxed local memory (SRAM) timing
  - Loosely coupled extensions using ROB

- First implementation
  - Fabricated by 65nm CMOS and can operate at 1GHz
Thank you!