Agenda

• The PNX8535, first pictures
• Application background
• PNX8535 functions and use cases
• PNX8535 device design
• Physical characteristics and key data
• Software support and tools
PNX8535, first silicon
Application background, integrated hybrid TV
Application background, integrated hybrid TV
PNX8535 functions and use cases

• Hybrid matrix television, for the ATSC/DVB market
  – Analogue and Digital broadcast reception and decoding
  – Conditional access (CableCard/CI)
  – A/V connectivity like:
    • Cinch/scart connections
    • HDMI/DVI input
    • VGA/DVI PC-inputs
  – Audio processing (volume, bass, virtualisation, Dolby SRS, etc.)
  – Video processing (de-interlacing, scaling, colour features, sharpening)
PNX8535 functions and use cases

• Output
  – Support for panels up to 1366*768@60p
  – Monitor/VCR output
  – Four stereo audio output DAC’s
  – Digital audio input/output (SPDIF)

• Use cases
  – HD/SD Analogue video/audio Input
  – HD/SD MPEG audio/video input/decode
  – HD/SD Digital video/audio input (HDMI)
  – PC Analogue Input
  – PC Digital Input via DVI/HDMI
  – FM radio
PNX8535 device design, video flow
PNX8535 device design, audio flow

- HDMI
- SPDIF-IN1
- TDA10046/60
- TS-IN
- Low-IF,SSIF
- L,R

PNX8535

- HDMI
  - HDMI Rx
- SPDIF-IN
  - SPDIF-MUX
  - SPDIF
- MC-U
- DigDEC-TM2270 (MPEG, AC-3 Decoder)
- DMA Bus
  - SPDIF-Out
- MUX
- Audio DSP (Post Processing)
- I2S I/O
  - Main L,R
  - HP L,R
  - Line/SCART2 L,R
  - SCART L,R

AAFE ADC
  - DemDec DSP (demodulation and decoding)
PNX8535 device design, control and compute
PNX8535 device design, MIPS – 4KEc core

• MTI Core 4KEc
  – MIPS32 Instruction set (release2), with MIPS 16e code compression
• Cache
  – 16KB Instruction
  – 8KB Data
  – 32 Byte line size
• CPU Pipeline
  – 5 Stage (Fetch, Execute, Multi/Divide, ALU, Write)
• Memory Protection
  – 32 entry joint TLB with 1KB page size
• Frequency
  – 240MHz (Worst Case)
PNX8535 device design, TriMedia – TM2270

• TM2270 core
  – TriMedia DSPCPU32 Level 3 Architecture
• Cache
  – 32KB Instruction, 128 Byte line size
  – 16KB Data, 64 Byte line size
• Pipeline
  – 5 Stage pipeline
  – 29 Functional units: Integer and Floating point ALU+DSP
• Frequency
  – 300MHz (Worst Case)
• Debug Support
  – Data and Code Breakpoints
PNX8535 device design, clock source

- External 27MHz Xtal
  - Used for Standby Controller
  - All clocks are division of 27MHz
  - Used for AVC System
    - Clocks are divided from $64 \times 27\text{MHz}=1.728\text{GHz}$ PLL
      - General clocks for IP e.g. UART, I2C, DCS,..
    - Clocks are generated from Direct Digital Synthesis
      - Fine adjustment for Audio/Video Streams
    - Clocks are multiplied by dedicated PLL
      - LVDS, DDR, MIPS
PNX8535 device design, clock architecture

CAB
- *64 PLL 1.728 GHz
- Dividers
- DDS *9
- PLL's
- DDR, MIPS, ....

CLOCKS
- 216MHz
- 102MHz
- ...

To IP

MMIO Control
PNX8535 device functional split in area

- Video Processing: 41%
- Periphery: 19%
- Audio Processing: 11%
- Infrastructure: 11%
- Computing: 9%
- AV Codec: 6%
- System Controller: 2%
- Connectivity: 1%
### PNX8535 physical characteristics- die

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Process</td>
<td>CMOS090HLV</td>
</tr>
<tr>
<td>Masks</td>
<td>34 (6 layer metal)</td>
</tr>
<tr>
<td>Transistors</td>
<td>~40 Million</td>
</tr>
<tr>
<td>Power</td>
<td>3-3.5 Watts</td>
</tr>
<tr>
<td>Analogue/Decap</td>
<td>20% of Core</td>
</tr>
<tr>
<td>Memory</td>
<td>25% of Core</td>
</tr>
<tr>
<td>Logic</td>
<td>55% of Core</td>
</tr>
<tr>
<td>Power Domains</td>
<td>3.3V, 2.5V, 1.2V</td>
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<tr>
<td>Clocks Domains</td>
<td>75</td>
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<tr>
<td>Wire diameter</td>
<td>25um</td>
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<tr>
<td>Bondpad Opening</td>
<td>50x70um</td>
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<tr>
<td>Pad Cells</td>
<td>750</td>
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<tr>
<td>Bond Fingers</td>
<td>515</td>
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<tr>
<td>Power Rails</td>
<td>30</td>
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<tr>
<td>Bond Wires</td>
<td>704</td>
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<tr>
<td>Package</td>
<td>BBGA 40x40mm</td>
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<tr>
<td>Ball</td>
<td>596</td>
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<tr>
<td>Signals Balls</td>
<td>416</td>
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<tr>
<td>Power Balls</td>
<td>144</td>
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<tr>
<td>Thermal Balls</td>
<td>36</td>
</tr>
<tr>
<td>Laminate</td>
<td>4 Layers</td>
</tr>
</tbody>
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Software support

<table>
<thead>
<tr>
<th>Conditional Access (Option)</th>
<th>De-multiplexer</th>
<th>MPEG Decoder Audio &amp; Video</th>
<th>Analog Front-End HDMI</th>
<th>Video Decoder &amp; 3D Comb</th>
<th>Audio Demdec</th>
<th>Audio post Processor</th>
<th>Video post Processor</th>
</tr>
</thead>
</table>

On-Chip Hardware

Software Stack
Software support

• Linux drivers
  – Standard drivers for all the different on board hardware peripherals
• Platform
  – Implements hardware independent API for higher levels of software.
  – Provides implementation of automatic behaviour like view modes, muting/blanking
• Middleware/User interfaces
  – Implementation of user functions like channel change.
Summary, conclusions

• PNX8535
  – Is a highly integrated hybrid television processor.
  – Combines high performance (high definition) audio/video decoding and processing in a single SOC.
  – Supports both a general purpose CPU (MIPS) as well as a dedicated media processor (Trimedia).
  – Combines software and hardware media processing in a single streaming framework