The Next Generation
65-nm FPGA

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Structure of the talk

• 65nm technology going towards 32nm
• Virtex-5 family
• Improved I/O
• Benchmarking Virtex-5 LUT6 fabric
• New Microblaze in Virtex-5 fabric
• Conclusion
65nm Process Technology

- 40-nm gate length (physical poly)
- 1.6nm oxide thickness (16 Angstrom)
  - ~5 atomic layers
- Triple-Oxide II technology
  - 3 oxide thicknesses for optimum power and performance
- 1.0 Vcc core
  - Lower dynamic power
- Mobility engineered transistors (strained silicon)
  - Maximum performance at lowest AC power

Over 1 Billion Transistors on a 23 x 23 mm Chip
FPGAs Drive the Process

New process technology drives down cost
FPGAs can take advantage of new technology faster than ASICs and ASSPs

FPGA 2010: 32 nm, 5 Billion transistors

The cost of IC development increases. Therefore customers want to buy reconfigurable and programmable platforms, instead of developing their own.
Challenges

• Higher leakage current and stand-by power
• Lower Vcc: good for power, tough for decoupling
  – 3.3-V compatibility is getting more difficult
  – 1 billion transistors, large chips, heat density
  – 12-layer chip, 10-layer package, 16-layer pc-board
• Faster transitions, 2 V/\text{ns} \quad \text{and} \quad 50 \text{ mA}/\text{ns} \per \text{pin},
  – Pc-board signal integrity problems

*Complex chip, complex package, complex board*
LX Platform
Overview
Two Generations of ASMBL
(Application-Specific Modular Block Architecture)

Virtex-4

Virtex-5
2nd Generation of ASMBL

Easy to create sub-families

- **LX**: Logic + parallel I/O
- **LXT**: Logic + serial I/O
- **SXT**: DSP + serial I/O
- **FXT**: PPC + fastest serial I/O

Many choices to optimize cost and performance
System components

- High-Performance 6-LUT Fabric
- 36Kbit Dual-Port Block RAM / FIFO with ECC
- SelectIO with ChipSync + XCITE DCI
- 550 MHz Clock Management Tile DCM + PLL
- 25x18 Multiplier DSP Slice with Integrated ALU
- More Configuration Options
Virtex-5 Logic Architecture

- True 6-input LUTs
  - with dual 5-input LUT option
  - 1.4 times the value for actual logic
  - only 1.15 times the cost in silicon area.

- 64-bit RAM per M-LUT
  - about half of all LUTs

- 32-bit or 16-bit x 2
  - shift register per M-LUT
Virtex-5 Routing

More symmetric pattern, connecting CLBs

More logic reached per hop

Same pattern for all outputs
BRAM/FIFO

• 36 Kbit BRAM
  – Integrated FIFO Logic for multi-rate designs
  – Built-in ECC
  – Cascadable to build larger RAM arrays
  – Dual Port: a read and write every clock cycle

• Performance up to 550 MHz
General Purpose I/O (Select I/O)

• All I/O pins are “created equal”
• Compatible with >40 different standards
  – Vcc, output drive, input threshold, single/differential, etc
• Each I/O pin has **dedicated circuitry** for:
  – On-chip transmission-line termination (serial or parallel)
  – Fine timing adjustment in 75 ns steps (IDELAY + ODELAY)
  – Serial-to-parallel converter on the input (CHIPSYNC)
  – Parallel-to-serial converter on the output (CHIPSYNC)
  – Clock divider, and high-speed “regional” clock distribution

*Ideal for source-synchronous I/O up to 1 Gbps*
75-ps Incremental Alignment

- Calibration clock can be internal or external
- 64 delay elements of ~70 to 89 ps each
ISERDES for Incoming Data

- Clock frequency division widens internal data path
  - \( n = 2, 3, 4, 5, 6, 7, 8, 10 \) bits
- Dynamic signal alignment
  - Bit alignment, Word alignment, Clock alignment
- Supports Dynamic Phase Alignment (DPA) using IDELAY
OSERDES for Outgoing Data

- Parallel-to-Serial converter
  - Data SERDES: 2, 3, 4, 5, 6, 7, 8, 10 bits
  - Three-state control SERDES: 1, 2, 4 bits
Virtex-5
Applications
Benchmarks
One MPEG4 Video Decoder

- High Definition resolution
- 720 vertical video lines, progressive
8 MPEG4 decoders

<table>
<thead>
<tr>
<th>Category</th>
<th>Virtex-4</th>
<th>Virtex-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tools</td>
<td>XST/ISE 8.1.02i</td>
<td>XST/ISE 8.2i</td>
</tr>
<tr>
<td>Devices</td>
<td>XC4VFX140-11</td>
<td>Virtex5 part</td>
</tr>
</tbody>
</table>
8 Decoders: Resources

- 35% fewer LUTs
- Dramatic improvements for multiplexers, memory, and misc. logic
- Same VHDL source code used for both designs

### Estimated FPGA Resources for Eight MPEG-4 Decoder Design

<table>
<thead>
<tr>
<th>Design Resources</th>
<th>Virtex-4</th>
<th>Virtex-5</th>
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<tbody>
<tr>
<td>Registers</td>
<td>21,248</td>
<td>20,242</td>
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<tr>
<td>LUTs</td>
<td>67,523</td>
<td>44,148</td>
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<tr>
<td>BlockRAMs</td>
<td>233</td>
<td>233</td>
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<tr>
<td>DSP Elements</td>
<td>192</td>
<td>216</td>
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</tbody>
</table>

Diff. = 6932
Logic Synthesis-Driven Results

- Synthesis uses 6-input LUTs efficiently: fewer logic levels
- 23% increase in synthesized frequency, from 95MHz to 117MHz
- From 720p to 1080p video standards with little effort
Quad-Port Memory in Four LUT6

- Write Port: Four LUT6s share the data input and can also share a distributed write address.

- Read Ports: Three independent read operations.

- 32 x 32 Quad-Port RAM structure in 64 LUTs.

- 6x density improvement over Virtex-4.
Application Example:
new MicroBlaze 5.0

- Better use of new LUTs
  - 1269 LUT4s in Virtex-4, MB 4.0
  - 1400 LUT6s in Virtex-5, MB 5.0
- from 3 stage -> 5 stage pipeline

- new processor: from 0.92 DMips/MHz to 1.14 DMips/MHz
- 180MHz -> 201 MHz
- 166 -> 230 Dhrystone Mips

Use new 6 LUT, 2 stage deeper pipe, 10% more MHz, 39% better performance
Suite of Benchmarks

Suite of 74 designs run against ISE8.1i
Slow speedgrade (-10) Virtex-4 compared to slow speedgrade (-1) Virtex-5

~30% average advantage for Virtex-5 fabric vs. Virtex-4
- As high as 56% advantage for some designs
Virtex-5: Summary

- Leading 65 nm technology FPGA platform
- Better input and output I/O on all pins
- New 6-input LUT logic that is 30% better
- Demonstrated example of video benchmark with 35% fewer LUTs and 23% increased frequency
- New Microblaze with 39% improved performance
- Expect more: new announcements on serial I/O and integrated processor technology very soon
Appendix: Virtex-5 LX
## Virtex-5 LX Platform

<table>
<thead>
<tr>
<th>Logic Cells</th>
<th>5VLX30</th>
<th>5VLX50</th>
<th>5VLX85</th>
<th>5VLX110</th>
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<tr>
<td>LUT6/FFs</td>
<td>30,720</td>
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