The APP300 Access Network Processor

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Target Market: Access Network

**Multi-Service Edge**
- Stable
- Very high performance
- Highest port density
- ATM, IP and MPLS services
- All optical (OC-n)

**Access Systems**
- Ongoing deployment
- ATM now, going Multiservice
- Access for business, residence, remote terminal
- SONET/SDH/PDH/Ethernet interfaces

**Customer Premise/Access**
- Emerging market opportunity
- Broadband on existing copper
- Integration play
- Last real network problem: delivery of high quality bandwidth on demand to “the masses”

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### Diagram

- **Metro Backbone Service Node**
- **Multiservice Packets**
- **Multiservice Data and Transport Platforms (MSSP/MSTP)**
- **Base Transceiver Station (BTS/Node B)**
- **Digital Subscriber Line Access Modules (DSLAM)**
- **Multiservice Access Nodes (MSAN)**

- **Residential/SoHo Access**
- **Remote Access DSLAM**
- **xDSL**

- **Business Access**
- **Remote Access Multi-Service**
- **NxE/T NxFE/GE**

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APP300
Agere’s approach

- Highly pipelined wire speed data path that is programmable
- Embedded Processor for Control processing

**Wire-speed Path**
- Forwarding
- Shaping
- Queuing
- SAR
- Monitoring, etc.

**Slow-speed Path**
- Connection setup
- Error processing
- Statistics reporting
- Configuration, etc.

*Image of a data path diagram with labels for Data Path and Control Path.*

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Alternative Approach #1

- Works well in simple systems
- Higher speeds, more functionality needed
- Starts falling behind dramatically
- Results vary dramatically with each software tweak

Array of Processor Cores

Data in

μP Core
μP Core
μP Core

Data out

Lookup Table
Program
Data Storage
Alternative Approach #2

- Develop custom ASIC to perform wirespeed routing/queuing
  - High development costs
  - Long time to market
  - No flexibility in an emerging market

**ASIC based approach**

![Diagram showing Custom ASIC, Lookup Table, and Data Storage]
Agere’s approach

Processing Steps:

- PHY
- Assem.
- Recog. Classify
- Queuing
- Traffic Shaping
- Packet Mod
- Seg.
- PHY
- Host Traffic
- Policing/Stats
- Host Processor
- Host Traffic
APP300 Block Diagram

- DDRII SDRAM
  - Reassembly and Packet Buffer
  - Program, DID and SED
- MAC Interface
  - Classification and Reassembly
    - Classification Engine
    - Queue Engine
  - Reassembly Buffer control
- Input Interface
  - ARM9
    - Statistics And Policing Engine
- DDRII SDRAM
  - Flash
- Output Interface
  - MAC Interface
    - GMII, SMII MAC
  - POSPHY / UTOPIA
- PORTS 0-3
  - POSPHY / UTOPIA
- PORT 4
  - Internal PORT 4 Loopback
  - PORT 5 Management Port
**APP300: Interface Configuration**

**Flexible Ports**
Enables simplified, lower cost solutions

- **Integrated ARM 926 Processor**
  - 200MHz
  - PowerQUICC 16-bit host intf
  - Supports Master & Slave Modes of operation

- **Peripheral Support**
  - I²C – 2 pin serial interface
  - SPI – 4-pin serial interface
  - UART, WDT, GPIO, JTAG
  - Interrupt Controller
  - 10/100 Ethernet interface for control path
Unified Memory Architecture

- All external Memories are DDR-II SDRAM. No expensive SRAMs or CAMs.
- All Control and data stored in three external Memories and internal memory (down from 6 FCRAMs and 5 DDR SRAMs in the previous architecture).
- Control Memory (DDR-II SDRAM, 16b): Stores Classification and Traffic Manager control structures.
- Data Memory (DDR-II SDRAM 16/32b): Stores PDU data.
- ARM Program Memory (DDR-II SDRAM 16b): Stores instructions and data for the control processor.
- Optional ECC protection on all external memories.
Unified Memory Architecture (contd.)

- **Internal Memory**
  - 828KB of Internal Memory shared between 8 clients
  - 32 chunks of memory – sizes 256KB, 128KB, 64KB, 48KB, 32KB, 16KB & 8KB
  - Configurable cross bar enables memory to be assigned to different clients in a programmable fashion
APP300 Overview - Classifier & Policing Engine

- Recognition/Classification/Filtering
- Functional Processing
- Assembly (if necessary)
- Policing and Statistics

Classifier


Policing/Stats

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APP300 Overview - Classifier & Policing Engine

**Features**

- Programmable classification up to Layer 7
- Functional Programming Language
- Highly pipelined parallel processing of PDUs
- ATM re-assembly
- Table lookup with millions of entries & variable entry lengths. On chip Tree Cache to speed up processing
- Configurable UTOPIA / POS interfaces
- Built in Receive MAC for Ethernet support

**Benefits**

- Time to market, ease of upgrade
- Reduces development time, code maintenance
- High performance scalable architecture
- Eliminates external SAR
- Eliminates need for external CAMs; deterministic performance regardless of table size
- Simplifies design and reduces system cost
- Programmable Policing and Statistics engine for flexibility
- OAM support in the Policing Engine

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APP300 Overview - Classifier

- Input Framer
- Buffer Control
- Output Interface
- Block Buffers and Context Memory
- Pattern Processing Engine
- Queue Engine
- Configuration Bus Interface
- Functional Bus Interface
- Tree Cache
- 8-bit Pos from State Engine
- GMII/SMII
- From PHY
- To Control DDR Interface
- To Internal Memory
- Functional Bus to Policing Engine
- 32-bit POS to Traffic Manager
- To Packet DDR Interface

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APP300 Overview - Traffic manager

- Transmit queuing
- Traffic Management and Shaping
  - Quality of Service (QoS), Class of Service (CoS)
- Packet Modification
  - Including Segmentation, CRC

Traffic Manager
APP300 Overview - Traffic Manager
APP300 Overview - Traffic Manager

**Features**

- **2K queues**
  - programmable shaping UBR, VBR, CBR
  - programmable discard policies
  - programmable QoS/CoS
  - 6 levels of scheduling hierarchy
- **Support for Multicast**
- **Highly pipelined processing of PDUs**
- **Generates required checksums/CRC**
- **Built in Transmit MAC for Ethernet support**

**Benefits**

- Large number of connections
- Support for emerging apps
- High performance architecture
- Smart processing at high bandwidth and low cost.
- Compute Engine processors for complete flexibility in Traffic Management, Shaping and Packet Editing
APP300 Overview - Traffic Manager

Input Interface
Assembly
Stream Editor
Output Interface

To DDR2 Packet Memory Interface
To DDR2 Control Memory Interface
Output Interface
To State Engine

32-bit bus from FPP
8-bit Configuration Bus

Context
Buffer Management
Transmit Request
Flow Control

To Internal Memory

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APP300 Overview - Scheduling Hierarchy

- **6 Output Ports**
- **256 Port Managers**
  - Port Manager rate specified. Sum of rates of port managers under an Output Port bound by Output Port Rate.
- **512 Logical Ports**
  - Multiple Logical Ports per Port Manager
- **1024 Schedulers**
  - Up to 4 schedulers per Logical Port.
  - Static (CBR), Dynamic (VBR) and FIFO (UBR)
  - Dynamic and FIFO schedulers under Script Control
- **2048 Queues** – QoS queues with up to 16 CoS queues
  - CoS Queue Scheduling under script control
APP300 Overview - Scheduler Details

Static Schedulers

- Q 55
- Q 36
- Q 55
- Q 104
- Q 55
- Q 36

Next Queue to Service

Software programs table in memory

Current Queue

Dynamic Schedulers

- Q 36
- Q 104
- Q 36

Current Queue

Traffic Shaper script writes the current queue into its next timeslot

HW handles multiple queues in a timeslot

FIFO Schedulers

- Q 36
- Q 75
- Pending 1
- Pending 2
- Pending 3

To penalty Box

Four lists – read queue from active list.
Queue can be re-inserted in Traffic Shaper script into any of the 4 lists or to a Penalty Box
HW handles multiple queues in a slot
APP300 Overview - Host Processor Subsystem

- **DDRII SDRAM**
  - Reassembly and Packet Buffer
  - Program, DID and SED
- **Ports 0-3**
- **Port 4**
  - ARM9
  - Host Bus I/F
  - ARM I/O
  - DDRII SDRAM
  - FLASH
  - Statistics And Policing Engine
  - 828K Internal Memory
- **Classification and Reassembly**
- **Statistics And Policing Engine**
- **Reassembly Buffer control**
- **Classification Engine**
- **Queue Engine**
- **PDU Assembler**
- **Stream Editor / Compute Engine**
- **RGB/Traffic Management Compute Engine**
- **General Purpose Packet Generator Engine**
- **Traffic Shaping Compute Engine**
- **828K Internal Memory**
- **828K Internal Memory**
- **828K Internal Memory**
- **GMII, SMI MAC**
- **Input Interface**
- **Output Interface**
- **MAC Interface**
- **POSPHY / UTOPIA**
- **POSPHY / UTOPIA**
- **POSPHY / UTOPIA**
- **PORTS 0-3**
- **PORT 4 Management Port**
- **GMII, SMI MAC**
- **PORT 4 Management Port**
APP300 Overview - Host Processor Subsystem

Features

- ARM 9 core – low silicon + royalty cost and adequate performance.
- DDR2 Memory, Ethernet and Flash interfaces
- Peripheral interface – GPIO, UART, I2C, SPI etc.
- Control packets to the Classifier and from the Traffic Manager
- Seamless Modem configuration through a Configuration interface

Benefits

- On chip ARM core can be as a controller. Build a system without using an external processor
- Can work with an external processor, if needed.
APP300 - IC Perspective

- 15.16mm x 10.17mm
- 6LM, 0.13um FSG CMOS
- 123 million transistors
- 12.9Mb memory
- 9 million logic gates
- 1.0V core, 1.8V & 3.3V IO
- 166MHz internal operation
- 200MHz DDR I/O operation
- ARM926EJS (200 MHz)
- SPI-3/Utopia 2,3/ POS-PHY2/GMII/SMII
- GPIO, FLASH, Host Port, RMII, UART, SPI, I²C
- 2 x 1GHz PLLs Circuit under Pad
- 744 PBGAMTH, 1.27mm pitch, 37.5mm body, heat spreader
APP300 Performance

- Advertised performance: 300 Mb/s – 2.25 Gb/s based on family member and configuration
- Maximum sustained throughput (with full classification and 5-level scheduling/shaping): 3.3 Gb/s
- Classification budget: Up to 192 bits/packet with 64 byte packets at full throughput
- Real world application performance example:
  - 64 modem full line rate ADSL2+ IP DLSLAM configuration
  - Full DSL Forum Working Text-101 compliant processing (including scheduling/shaping)
  - Real-world traffic mix
  - 100% throughput with zero packet loss and headroom to support 72 port ADSL2+ configurations and 48 port VDSL configurations
APP300 Based DSLAM Solution

**APP300 Features**
- AAL5 SAR (2K simultaneous reassemblies)
- Up to 2K Queues
- ATM scheduling (CBR, VBR, UBR)
- Frame Scheduling (GFR, programmable)
- Asymmetrical Processing
- 2G or 1.2 G throughput
- Embedded Control Plane Proc (ARM)
- Low cost BOM for complete Ethernet DSLAM
- Data plane code for Supporting Ethernet
- 802.1q,p, 802.3 ad, VLAN etc.

Direct DSL Modem interface
- UTOPIA-2 MPHY
- 8 or 16 bit
- Full I.610 OAM
- Available POS-2, POS-3
## APP300 Summary

### Interface Flexibility
- Multiple interface options allow support of a variety of physical layer devices

### Powerful Processing
- Patented classification & traffic management algorithms
- Hierarchal scheduler
- Wire-speed, deterministic performance
- ATM, MPLS, IPv4/v6, Ethernet

### Scalability
- Covers entire application range from 600Mbps to 2 Gbps

### Low BOM cost
- Embedded host processor, Low cost memory, PCB-friendly pinout to minimize board layers

### Powerful and efficient programming model
- Hardware-optimized classification and pattern matching language
- Concise scripts implement powerful algorithms
- Dramatically reduced total cost of ownership