Inside Intel® Core™ Microarchitecture

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Agenda

Processors and main specifications
Performance data
Intel® Core™ Microarchitecture Overview
The Level 1 Memory subsystem
  Structures and dimensions
  Memory order buffer and Memory Disambiguation
  Prefetchers
  Shared L2 cache

Summary
What is Intel® Core™ Microarchitecture?

The Intel® Core™ Microarchitecture is a new foundation for Intel® architecture-based desktop, mobile, and mainstream server multi-core processors. It is designed for efficiency and optimized performance across a range of market segments and power envelopes.

2006 Intel Core Microarchitecture based processors:

**DP Server:**
Dual-core Intel® Xeon® 51xx Processors
Quad-core codenamed Clovertown

**Desktop:**
Dual-core Intel® Core™ 2 Duo Processors
Quad-core codenamed Kentsfield

**Mobile:**
Dual-core Intel® Core™ 2 Duo Processors

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What is Intel® Core™ Microarchitecture?

The Intel® Core™ Microarchitecture is a new foundation for Intel® architecture-based desktop, mobile, and mainstream server multi-core processors

**Designed for efficiency and optimized performance across a range of market segments and power envelopes**

<table>
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<th>65nm</th>
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<td>Die size:</td>
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<td>Transistor count:</td>
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<tr>
<td>Execution core area:</td>
<td>36 mm²</td>
</tr>
<tr>
<td>Execution core transistor count:</td>
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</tr>
</tbody>
</table>

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## Product specifications (Preliminary)

A variety of products with different specs will be available

<table>
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<tr>
<th>Spec</th>
<th>Codename</th>
<th>Xeon™ 5100 servers</th>
<th>Core™2 Duo desktops</th>
<th>Core™2 Duo mobility</th>
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<tr>
<td>Max frequency</td>
<td></td>
<td>3.00 GHz</td>
<td>2.93 GHz</td>
<td>2.50 GHz</td>
</tr>
<tr>
<td>Max Front Side Bus frequency</td>
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<td>1.066 GT/s</td>
<td>0.667 GT/s</td>
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<tr>
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<td></td>
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<td>75 W for the 2.93Ghz version, 65 W for lower frequency versions</td>
<td>34 W</td>
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<tr>
<td>Max VID</td>
<td></td>
<td>1.325V</td>
<td>1.325 V</td>
<td>1.300 V</td>
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</table>

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The Intel Core 2 Duo E6700 delivers +40% performance while requiring +40% less power than the Pentium D Processor 960.
Extreme Gaming
Intel® Core™2 Duo Processor:

Intel® Pentium® Processor Extreme Edition 965 (2x2MB L2, 3.73GHz, 1066MHz FSB) with dual graphics

Intel® Core™2 Extreme Processor X6800 (4MB L2, 2.93GHz, 1066MHz FSB) with dual graphics

Games used medium settings and 1024x768x32 resolution. These settings are used for comparing CPU contribution to game performance.

Source: Intel. Configuration: Processor as listed above, Intel 975X Express Chipset on Intel D975XBX board, Intel chipset software installation file 7.2.2.1007, Intel Matrix Storage Manager 5.5.0.1035 RAID-0 Ready, Dual ATI® Radeon® X1900 XTX PCIe, ATI Catalyst Driver 6.6 driver 8.263.0.3, 2x1GB OCZ® DDR2 800 4-4-4-12, Maxtor® DiamondMax® 10 300GB NCQ Serial ATA 7200RPM, Windows® XP Professional Build 2600 SP2 NTFS, DirectX 9.0c. Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, visit http://www.intel.com/performance/resources/index.htm

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Intel® Core™ Microarchitecture - Overview

Instruction Fetch And PreDecode

Instruction Queue

Decode

Rename/Alloc

2M/4M Shared L2 Cache
Up to 10.6 GB/s FSB

uCode ROM

Retirement Unit (ReOrder Buffer)

Schedulers

ALU Branch MMX/SSE FPmove
ALU FAdd MMX/SSE FPmove
ALU FMul MMX/SSE FPmove
Load
Store
Memory Order Buffer

L1 D-Cache and D-TLB

Intel® Wide Dynamic Execution

Intel® Advanced Digital Media Boost

Intel® Smart Memory Access

Intel® Advanced Smart Cache

Intel® Intelligent Power Capability
Intel® Wide Dynamic Execution

- 4 (5) wide decode
- 4 wide rename
- 4 (5) wide retire
- 5 (6) instructions/clock
- 32 entry scheduler (32 micro-ops considered for dispatch each cycle)
- Deep out of order storage

33% Wider Than Previous Generations
**Intel® Wide Dynamic Execution (cont ..)**

**Extended Stack Pointer (ESP) tracker**
- Stack Pointer updated by dedicated hardware
- SP BW increased by 33% over Core™ Duo processor

**Micro-Op Micro-Fusion**
- Single Uop representation of “multi-uop” instruction
- 4 instructions per cycle
- Extended to additional cases
Intel® Wide Dynamic Execution (cont ..)

**Macro-Fusion**

- Represent most frequently used IA32/Intel® 64 instruction pair as single micro-op

- Enhanced Arithmetic Logic Unit (ALU) for macro-fusion
  - To execute new compare and jump (CMPJCC) micro-op in one clock
Intel® Advanced Digital Media Boost

128-bit packed Add

plus

128-bit packed Multiply

plus

128-bit packed Load

plus

128-bit packed Store

plus

eone Integer instruction (e.g.: a CMPJcc)

2x Compute Throughput / Clock
Intel® Smart Memory Access

Instruction Fetch
And PreDecode

Instruction Queue

Decode

Rename/Alloc

Retirement Unit
(ReOrder Buffer)

2M/4M Shared L2 Cache
Up to 10.6 GB/s FSB

Memory Disambiguation

Improved Prefetchers

Hiding Latency of Memory Subsystem
L1 memory subsystem – arrays dimensions

32 KB Write Back data cache
- 64 sets x 8 ways
- 64 byte/line in 8 banks
- Tag array dual ported

8 Line Fill/Write Combining buffers
- 4 Write Back buffers

Page Miss Handler

Data Cache Unit

Page Directory Entry $ 8x4

4K page array

Large page array

L0 4x4 * 4x4

L1 64x4 8x4

Load Buffer
- 32 entries

Store Buffer
- 20 entries

Memory Order Buffer

* sets X ways

Data TLB
Example of basic MOB's ordering operation

- **Direction of dependency check**
  - **Tail** (oldest)
  - **Head** (newest+1)

- **SB**
  - ST 1
  - ST 3

- **Range for dependency and unknown address checks**

- **Store color of LD 2 defined as store preceding LD 2**
  - LD 2 needs to check all stores from store_color back up to tail
  - If a match found => forward

- **A series of uOps in program order**
  - ST 1 (100h)
  - ST 2 (500h)
  - ST 3 (200h)
  - LD 2 (100h)
  - ST 4
  - ....
MOB operation with Memory Disambiguation

A series of uOps in program order

| ST 1 (100h) |
| ST 2 (500h) |
| ST 3 (200h) |
| LD 2 (100h) |

Predict if LD 2 can proceed despite unknown stores (ST 2)

If predicted colliding: act as without disambiguation (i.e. block it if store address unknown)

If predicted non colliding:
- Let the load proceed even if unknown store address
- If actually colliding, restart the load and all successive instructions
Without Memory Disambiguation

Instruction using Data X is almost ready to go, all it needs is X from memory.
Without Memory Disambiguation

Store Buffer

Data W
Data Z
Data Y
Data X

1 Data Y is stored First

Load4
Store3
Load2
Store1

X
W
Y
Y

Oldest
Without Memory Disambiguation

1. Data Y is stored First
2. Followed by load of Same cache line
Without Memory Disambiguation

Store Buffer

1. Data Y is stored First
2. Followed by load of Same cache line
3. Data W Store Next

Load4: X
Store3: W
Load2: Y
Store1: Y

Oldest
Without Memory Disambiguation

1. Data Y is stored first.
2. Followed by load of same cache line.
3. Data W store next.
4. Finally load of X takes place.
With Memory Disambiguation

Lolds can decouple from Stores.

Load4 can get its data FIRST
With Memory Disambiguation

Memory Disambiguation enables Load4 to go earlier
- The dependency shadow of Load4 starts executing earlier
With Memory Disambiguation

Memory Disambiguation enables Load4 to go earlier
- The dependency shadow of Load4 starts executing earlier

Store of Y can now take place and does not delay any other instructions
With Memory Disambiguation

Memory Disambiguation enables Load4 to go earlier
- The dependency shadow of Load4 starts executing earlier

Store of Y can now take place and does not delay any other instructions

Load of Y is next
With Memory Disambiguation

Memory Disambiguation enables Load4 to go earlier
- The dependency shadow of Load4 starts executing earlier

Store of Y can now take place and does not delay any other instructions

Load of Y is next

Store of W is last
How is the prediction done?

- Using an history array indexed by Instruction Pointer
- An entry in the history array consists of a saturating counter
- When a particular load “failed” or “would have failed” disambiguation: reset its counter
- Each time a particular load could have been correctly disambiguated: increment counter
- If counter saturates: disambiguation possible on this load (starting from next iteration)
How is the prediction verified against the actual outcome?

- History update done at load’s retirement based on control bits in the Load Buffer

- When a store is executed, scan all younger loads in the Load Buffer and mark conflicting cases:
  - Predicted colliding / actually colliding => reset
  - Predicted not colliding / actually colliding => reset, restart

- Disambiguation is disabled/suspended in some cases, either to enforce ordering, for implementation reasons, or to prevent performance loss
High level view of prefetchers

Legend

Request Destination
Trigger source

Prefetch related logic

L2 streamer

L2 prefetcher (16 entries)

FIFO

DCU streamer

IP prefetcher

Line Fill Buffers (LFB)

L1 data cache (32K)

L2 cache (4M)

L1 code cache (32K)
Map of Prefetchers and Multi-core
Intel® Advanced Smart Cache

Dynamic Cache Allocation:
Shared cache enables each core to have access to full cache for faster data access.

Large Shared Cache:
Only one copy of shared data is kept in the cache and can be accessed by both cores.

Dynamic Bandwidth Allocation:
High bandwidth application can borrow L1 to L2 bandwidth from the other core’s application.

2X L2 to L1 Bandwidth
Sustained rate of 2 cycles per cache line
Summary

Intel® Core™ Microarchitecture is a new foundation for Intel® architecture-based mobile, desktop, and server processors

Incorporates advanced innovations which optimize performance over a range of market segments. Among them:

• Memory disambiguation increases performance by eliminating false memory dependencies, improving latency associated with memory accesses
• Advanced prefetchers successfully place data in caches for “just-in-time” execution, hiding memory latencies
• Advanced Smart Cache provides flexible performance for both single and multi threaded applications

A microarchitecture which delivers increased energy efficient performance
Links

**Intel® Core™ Microarchitecture:**
http://www.intel.com/technology/architecture/coremicro/

**Intel® Energy-Efficient Performance:**

**Intel Product Benchmark Details:**
http://www.intel.com/performance
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