Transcend™

Solving 4G Challenges for Pico, Micro and Macrocell Platforms

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Communications Convergence Processing
Mindspeed Technologies, Inc.
The Next Internet Wave – Mobility and Content

Innovative New Platforms

New Networked Applications

≡ Explosive demand for Mobile Broadband
Impact on Service Providers

... Overloaded Networks

Source: Infonetics Q4'2009

Source: 2010 Cisco VNI Mobile
2G to 4G - System Architecture Evolution - to the Evolved Packet Core

- **2G GSM** – 1990s
  - BTS
  - Node B
  - eNode B

- **3G W-CDMA** – 2000s
  - TRAU
  - RNC
  - SGSN
  - GGSN

- **4G LTE** - 2010
  - Mobility Management
  - aGW
  - Media GW
  - Video processing
  - Speech Codec
  - Voice band data

- **Mobile Operator Core Network**
  - Packet Switching

- **Networks**
  - Packet Switching

- **Media**
  - Video
  - Speech

- **Evolution**
  - From 2G to 4G
  - System architecture
  - Evolution to the Evolved Packet Core

- **Technologies**
  - TDMA
  - CDMA
  - OFDMA
  - MIMO
  - MMX
  - Security
  - QoS
  - Mobility Management
  - Voice band data
  - Media GW
  - IP Packet
  - ATM Cells/TimeSlots

- **Standards**
  - 2G GSM
  - 3G W-CDMA
  - 4G LTE
Mobile Broadband Architecture – Going Distributed

Serving a broad range of basestations - from Macro to Femto

1200
Supported Subscribers

400
High-Density Subs

200
Business

50
Enterprise Femto

10
Residential

Macro
Micro
Pico
Metro
Urban
High-Density Subs
Business
Residential
Femto
Mindspeed SoC Competencies

Multi-Processor Communications Technologies
- Algorithms
- Standards Certification

Multi-Core Software
- Software Verification
- Software Architecture

Convergence Applications
- Packet Processing
- Voice, Video, and Modems
Silicon Architecture Evolution
Silicon & System Architecture Innovation

Old BTS Solutions
- T1/E1-ATM
- Abis
- Network Processors
- DSPs
- FPGAs
- IQ - Proprietary

Application Agnostic Component Architecture Solution

eNodeB Protocol Stack
- Ethernet
- IP
- LTE RRC
- LTE PDCP
- LTE RLC
- LTE MAC
- LTE PHY
- IQ - CPRI

System Architecture Evolution

Application Specific Architecture Solution

Transcede™ eNodeBs SoCs
- Ethernet
- IP
- Cipher
- RoHC
- Cortex A9s
- FEC
- CevaX
- FFT
- RAKE
- IQ - CPRI

Silicon Architecture Evolution
Transcede™ Dramatically Reduces System BOM

... while significantly accelerating Time-to-Market
eNB Transcede™ - Multi-Core SoC

- **High Performance DSP Farm**
  - SPU Cluster (10 SPU's)
  - Ceva X1641 MAP
  - Multi-Layer Non-Blocking AXI Bus

- **High Performance SERDES IO**

- **NoC: AXI Packet Network on Chip**

- **Intra-System Bridging**

- **High Performance SMP RISC**
  - System Cluster
  - ARM Cortex A9
  - AXI41 MII
  - ARM11 MII
  - AXI1 Bus
  - Memory to Memory DMA
  - DDR Core
  - DDR 2/3 PHY

- **Expansion System**

- **General Purpose Peripherals**

- **T4000:**
  - 600MHz/300MHz
  - T4020:
  - 750MHz/366MHz

**Key Features**
- Multi-Core SoC
- High Performance SERDES IO
- AXI Packet Network on Chip
- High Performance DSP Farm
- High Performance SMP RISC
- NoC: AXI Packet Network on Chip
- Intra-System Bridging
- General Purpose Peripherals

**Manufacturers**
- MNDSPACE
  - Build it First
  - Nasdaq: MSPD
### Processors: Instruction and Data Level Parallelism

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Processors: Instruction and Data Level Parallelism

Symmetric Multi-Core Instruction Parallelism

High Core Level Instruction Parallelism
Control/Branch Code Focus

Cortex-A9 CPU
600MHz to 750MHz **CevaX1641** 8-way VLIW DSP

- **600MHz to 750MHz Operation**
- **256bit-8 Way VLIW DSP**
  - 8-32bit Parallel Instructions
  - Most common size
  - 16-16bit Parallel Instructions
- **128bit 4/8 MAC SIMD**
  - 4-16bit x 16bit MACs
  - 8-8bit x 8bit MACs
- **Large L1 Memories**
  - 96kB Program RAM
  - Direct Mapped Cache Option
  - 128kB Data RAM
  - Banked Simultaneous Access
- **On-chip Emulation Module**
  - Complex Breakpoints/Trace/etc.
- **Dual Data/Program DMA/Cache**
- **Extensive Tool Chain**
  - C-Compliers/Debugger/etc.
Mindspeed Application Processor

Programmable Application Specific Signal Processing

General Purpose Signal Processor
- CevaX Core
- 62.5% RAM, 37.5% Core
- L1 RAM
- L1 RAM

Application Specific Signal Processor
- MAP Core
- 45% RAM, 55% Core
- L1 RAM
- L1 RAM

Fixed Function Signal Processing
- FFT/DFT Core
- 35-40% RAM, 60-65% Core
- L1 RAM
- L1 RAM

Limited Savings For Loss In Application Flexibility

Simplified Instruction Pipeline
Limited Control Code Focus
Small PRAM, L1 sized to limited function focus

No Instructions
State Machine Control
RAM sized to one function

Limited Savings For Loss In Application Flexibility
Mindspeed Application Processor (MAP)

- 600MHz to 750MHz Operation
- 160bit-1 Way VLIW DSP
- 160bit 4 MAC SIMD
  - 4- 24bit x 16bit MACs
- Built in FFT Radix Support
  - Bit Reverse Addressing
- Circular Buffering
- Built in Byte Data RAM read
- Very Wide/Large L1 Memories
  - 10kB Program RAM,
  - 80kB Data RAM
  - Banked Simultaneous Access
- External Sequencer Control
- High Performance DMA for Data
- 4G/3G Application Library
CoreSight™ SoC HW SW Debug Support

3G WCDMA HSPA+ & 4G OFDMA LTE PHY

Cortex A9 MP CPU

600-750MHz A9 CPU
- 32kB ICache
- 32kB DCache

600-750MHz A9 CPU
- 32kB ICache
- 32kB DCache

MP Technology-SCU

Cross Trigger Matrix

Trace Buffer Interface Unit

325kB ECC SRAM

Mux

Slave Port 6

Slave Port 4

Master Port 5

Slave Port 5

300MHz 64bit 7-Layer SYS_AXI

RealView
Tools by ARM®

Tightly coupled MAC/PHY
Streaming Real-Time Debug Capability!

Cortex
Intelligent Processors by ARM®

MNDSPED
BUILD IT FIRST™

Nasdaq: MSPD
Transcede™ 4000 SoC

- TSMC 40G Process 0.9V
- 12W typical
- 31mm x 31mm
- 26 Processors
- 9.1MBytes RAM
- >300M transistors
Multi-SoC Chaining in eNB Cells

- Each T4k is Chainable to other T4ks
  - Shared Inter-T4k Memory Maps
    - sRIO based HW Bridges
    - T4k(s) Share DDR, SRAM, IO, etc.
  - sRIO Mailbox System For Control
  - sRIO AXI DMA for Data Transfers

- T4k(s) can chain between eNodeBs
  - Create a eNB optical X2 interface
    - sRIO or VPN GigE

- T4k Distributed Antenna Systems
  - CPRI 5.0 up to 20km
  - Between BBU and RRH @ 10GT/s

Chainable Processing Tiles (Optical-20km or Electrical-20cm)
Seamless Scalability (Switchless)
Resulting In Lowest: Power, Cost, Area
Software Architecture Evolution
Mobile Data Link Standards Evolution

**2G**
- EDGE
  - DL: 474 kbps
  - UL: 474 kbps

**3G**
- HSPA
  - DL: 14.4 Mbps
  - UL: 6.78 Mbps
  - In 5 MHz
- Rel 7 HSPA+
  - DL: 28 Mbps
  - UL: 11.6 Mbps
  - In 5 MHz
- Rel 8 HSPA+
  - DL: 42 Mbps
  - UL: 11.6 Mbps
  - In 5 MHz
- Rel 9 HSPA+
  - DL: 84 Mbps
  - UL: 23 Mbps
  - In 10 MHz

**4G**
- LTE
  - DL: 306 Mbps
  - UL: 66 Mbps
  - In 20 MHz
- LTE (Rel 9)
  - DL: > 1 Gbps
- LTE Advanced
- Multi-Standard Drives eNB to Software Defined Radio (SDR) Architecture For HW Reuse

**CDMA2000**
- EV-DO Rev A
  - DL: 5.1 Mbps
  - UL: 1.8 Mbps
  - In 1.25 MHz
- EV-DO Rev B
  - DL: 14.7 Mbps
  - UL: 4.9 Mbps
  - In 5 MHz

**Fixed WiMAX**
- Fixed WiMAX

**Mobile WiMAX**
- Release 1.0
  - DL: 46 Mbps
  - UL: 4 Mbps
  - 10 MHz 3.1 TDD
- Rel 1.5
- IEEE 802.16m

Notes: Throughput rates are peak theoretical network rates. Radio channel bandwidths indicated.
Dates refer to expected initial commercial network deployment except 2008, which shows available technologies that year.
Innovation in Multi-Core Programming

C language dominates today's and tomorrow's sequential programs

However, C is a sequential language, so how do application developers map their C code into multi-core SoCs?

New modeling approach allows application partitioning and profiling early on in the design phase.

Task Dependencies
Sys HW params
Deadline (latency)
Rqrd. DSP Resources
List of Tasks
Task MIPS
Pass/Fail Indication

Task Composer Tool

Task List

SOURCE: Techie's 2009 Embedded Market Study
Software Multi-Core HW Mapping: LTE PHY & L2
Software Multi-Core HW Mapping: LTE PHY

PHY TASKS

FFT0  iDFT0
FFT1  iDFT1
RACH0  DL FEC 0
RACH1  UL FEC 0
UL SIC  IO Move

Control Plane: High Instruction Level Parallelism

Data Plane: High Data Level Parallelism

Optimized Match of Instruction and Data Parallelism
Key Differentiators of the Transcede™ Family

- Software configurable for all flavors of LTE, W-CDMA and WiMAX (SDR)
  --- Supports China standards, including TD-SCDMA and TD-LTE
- Significantly reduces system bill of materials
- Integrated L2 and L1 on a single SoC provides lowest possible latency
- Simplified programming model allows easy adaptation
- Roadmap of scalable SoCs delivers a range of performance/cost points across the range of base stations