3-D Stacking Tutorial
Introduction

Liam Madden
Corporate Vice President
Xilinx
Aug 27th 2012
Dedicated to the Memory of Chuck Moore: Visionary

Chuck Moore,
AMD Corporate Fellow
1961-2012
**Agenda**

- **Introduction**: Liam Madden, Corp VP, Xilinx (2:00-2:15)
- **Technology**: (2:15-3:05)
  - Foundry: Remi Yu, Director Marketing, UMC
  - OSAT: ChoonHeung Lee, Corp VP, Amkor
- **Design Considerations**: (3:05-3:55)
  - Mobile Communications: Riko Radojcic, Director, Qualcomm
  - FPGA: Shankar Lakka, Director Integration, Xilinx
- **Break**: (3:55-4:10)
- **System Implications**: (4:10-5:00)
  - Processor and GPU: Bryan Black, Senior Fellow, AMD
  - Integrated Optics, Ephrem Wu, Senior Director, Xilinx
- **5:00-5.30 Panel Discussion**
Cost Comparison: Monolithic vs Multi-Die

“Moore’s Law is really about economics” Gordon Moore
Why is first 3D logic product an FPGA?

- Natural partition using “long lines”
- Very low “opportunity cost”
- No 3rd party dependence
- “Size matters” to customers
- Compelling value proposition “next generation density in this generation technology”
Virtex 2000T: Homogeneous 2.5D

FPGA Slices Side-by-Side

Silicon Interposer:
>10K routing connections between slices
~1ns latency
Elements of SSIT

- **Silicon Interposer**
- **Microbumps**
- **Through-Silicon Vias (TSV)**

**Package Substrate**

- **28nm FPGA Slice**
- **C4 Bumps**
- **BGA Balls**

**Microbumps**

- Access to power / ground / IOs
- Through-silicon Vias (TSV)
  - Only bridge power / ground / IOs to C4 bumps

**Side-by-Side Die Layout**

- Minimal heat flux issues

**Passive Silicon Interposer (65nm Generation)**

- 4 conventional metal layers connect micro bumps & TSVs

**New!**

- **FPGA**
- **Package Interposer**
- **Microbumps**

**Package**

- 1mm
- 0.04mm
- 0.2mm

**Package Ball**

- 1mm
# 3 Decades of Microprocessor Integration: A personal history

“Integrate or be integrated”  Fred Webber, former CTO AMD

<table>
<thead>
<tr>
<th>Year</th>
<th>Company</th>
<th>Product</th>
<th>Integration Level</th>
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<td>FPU</td>
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What happened to System on a Chip?

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<th>Logic</th>
<th>Memory</th>
<th>Analog</th>
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<tr>
<td>Global Revenue 2011</td>
<td>$150B</td>
<td>$68B</td>
<td>$45B</td>
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<tr>
<td>Moore Scaling</td>
<td>Good (except I/O)</td>
<td>Good (except I/O)</td>
<td>Poor</td>
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<td>Technology “Vintage”</td>
<td>2012</td>
<td>2012</td>
<td>2000</td>
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<td>Transistor Characteristics</td>
<td>High performance/ Low leakage</td>
<td>Low leakage/ moderate performance</td>
<td>Stable with good voltage headroom</td>
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<td>Metallization</td>
<td>&gt;9 layers</td>
<td>&lt;5 layers</td>
<td>&lt;6 layers</td>
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<td>Differentiators</td>
<td>High density logic</td>
<td>Charge storage</td>
<td>Passives, Optical</td>
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Crossing the packaging chasm

Logic Process

Memory Process

Analog Process

DRAM Memory

Analog

uP

XILINX®
7V580T – Dual FPGA Slice with 8x28Gb/s SerDes Die

Virtex-7 HT @ 28Gbps