Foundry TSV Enablement
For 2.5D/3D Chip Stacking

Remi Yu, UMC
Hot Chips 24
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Outline

- 2.5D/3D Applications
- Foundry TSV Enablement
- Ecosystem Work Flow
- Summary
2.5D/3D Applications
2.5D Si Interposer Stacking

- Logic/logic: FPGA, networking infrastructure
- Logic/memory: Gaming, HPC
3D Logic/Memory Stacking
- Via-Middle TSV 28nm Logic + Memory Cube

- Mobile WideIO, Computing WideIO, HMC
Application Examples
- More are being developed

(3) eSilicon, “GSA 3D Working Group”, July 2012
Cost-of-Ownership Advantages

Motivations:
- Higher BW, lower W/BW, smaller form-factor

Opportunity of return on 3D IC investment:
- Chip process node optimization
  - Homogeneous partition
  - Cross-node combinations
- BOM cost optimization
  - Less demanding substrate/PCB, lighter cooling assembly, ...
- Ultimately: better product, better margin

Foundry TSV Enablement
Foundry TSV Process Technology

- Mainstream: Via-middle Cu TSV
  - 2.5D: 65nm-generation BEOL
  - 3D: 28nm CMOS logic

- After 28nm entry, TSV for 3D may come as a standard option for foundry CMOS logic at 20nm and beyond
Example TSV Unit Cell
- Via-Middle TSV for 3D

TSV Unit Cell
Cross-Section View

(drawn not to scale)

- TSV formed after CMOS, before contact/metal
UMC 28nm 3D IC

(CMOS device and TSV in proportion)
UMC Via-Middle TSV Unit Process

- Leveraging existing CMOS tools and capability
- Size is new to fab practice: diameter/depth
Early Stage TSV Process Issues

- TSV integrity – Cu fill, oxide liner, metal stack
ECP Cu Fill Process Optimization
- Cu pumping reduction

■ ECP Cu plating critical to TSV integrity
UMC Via-Middle TSV Solution

UMC via-middle TSV: void-free Cu gap fill
## TSV Top Side Impact Evaluation
### - BEOL WAT testkeys

<table>
<thead>
<tr>
<th>WAT test item</th>
<th>Layer</th>
<th>Testkey rule (w/s)</th>
<th>Above TSV</th>
<th>Cross TSV</th>
<th>Beside TSV</th>
<th>After Sinter</th>
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</thead>
<tbody>
<tr>
<td>Metal Bridge</td>
<td>M3</td>
<td>1xW/1xS</td>
<td>Passed</td>
<td>Passed</td>
<td>Passed (min. x=1)</td>
<td>No significant change</td>
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<tr>
<td></td>
<td>M4</td>
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<td>Passed (min. x=1)</td>
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<tr>
<td></td>
<td></td>
<td>2xW/2xS</td>
<td>Passed</td>
<td>Passed</td>
<td>n/a</td>
<td></td>
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<tr>
<td>Metal Resistance</td>
<td>M3</td>
<td>1xW/1xS</td>
<td>Passed</td>
<td>Passed</td>
<td>Comparable for variable x</td>
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<tr>
<td></td>
<td></td>
<td>2xW/2xS</td>
<td>Passed</td>
<td>Passed</td>
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<td></td>
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<td>2xW/2xS</td>
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<td>Passed</td>
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<td>Passed</td>
<td>Passed</td>
<td>Comparable for variable x</td>
<td></td>
</tr>
</tbody>
</table>

- Routing over TSV allowed
TSV Bottom Side Impact Evaluation

- Leakage CDF

Leakage effectively reduce

5K TSV Array Leakage CDF Chart

TSV process optimization improved Cu pumping and TSV/Sub leakage
CMOS Impact Evaluation (3D)  
- Keep-Out Zone (KOZ) Characterization

KOZ: Dlon< 3% at distance >=5um
- Device: 28nm HKMG core device
- TSV pitch: JESD229 50/40um
Via Middle TSV (3D)
- 6um diameter, 54um depth
Si Interposer TSV (2.5D)
- 10um diameter, 100um depth
Uniformity Evaluation
- 2.5D Si Interposer, 10x100um

Standard Deviation = 0.2um
UMC 3D IC TV Stacking & Package

Wide IO DRAM-DC

UMC: 28nm Logic

JEDEC WideIO interface

Diagram showing
- DRAM –DC
- ubump
- TSV
- Logic-CMOS
- Cu Pillar
- Substrate
Ecosystem Work Flow
Example 2.5D Stacking Flow
## Various Work Models

<table>
<thead>
<tr>
<th></th>
<th>FEOL</th>
<th>MEOL</th>
<th>BEOL</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Logic, TSV + FS RDL</td>
<td>Wafer Thinning, BS RDL + Bump</td>
<td>Assembly, Test</td>
</tr>
</tbody>
</table>

### Service scopes distinguished by MEOL inclusion
- Consult your foundry/OSAT

### Work flow optimization may depend on BOM cost, stack recipe and test strategy
### Foundry TSV Design Collaterals

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Feature Size</th>
<th>Document Status</th>
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<tbody>
<tr>
<td></td>
<td>TSV CD/Depth (um/um)</td>
<td>Topologic Layout Rule</td>
</tr>
<tr>
<td>1.0um-wide</td>
<td>10/100 (1.00/1.00)</td>
<td>Ready</td>
</tr>
<tr>
<td>0.4um-wide</td>
<td>10/100 (0.40/0.40)</td>
<td>Ready</td>
</tr>
<tr>
<td>0.56um-wide</td>
<td>10/100 (0.56/0.56)</td>
<td>Ready</td>
</tr>
</tbody>
</table>

(UMC 2.5D Si interposer documents)

- Consider TSV a passive device with rule decks/models
  - Typical foundry engagement applies under ecosystem work flow
UMC Ecosystem Effort

1Q12
- Foundry TSV process optimization

2Q12
- MEOL flow & QA alignment

3Q12
- MEOL 2.5D/3D chip stacking

4Q12
- Product level packaging & testing
- Reliability assessment
Summary

- Foundry TSV process demonstrated
  - Applicable to both 2.5D/3D
  - Leverage existing CMOS process technology
  - Key process issues identified & conquered

- Ecosystem work flow
  - Typical foundry/OSAT engagement flow applies for both 2.5D/3D, among other models

- Foundry TSV next step: ecosystem focus
  - Product level reliability assessment
  - Potential EDA collaboration for emerging 3D tools
Thank you for your attention!

Contact foundry@umc.com or info@hotchips.org.
Thank You!