Hot Chips: Stacking Tutorial

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Technology HQ, Amkor
Mobile Phone Technology Change

Feature Phone


Smartphones take lead in European mobile phone market
Simple 'feature phones' now make up less than 50% of sales as quarterly smartphone shipments exceed those of more basic devices for the first time

Smartphone

Source: in-stat, 2011

Smartphones as a Percentage of All Phones

Samsung SPH-B3650

FBGA
QFN
SSOP

FBGA
QFN
WLCSP
PoP
MEMS

Apple iPhone4S

Source: www.ifixit.com

Smaller & Thinner
PC Technology Change

Desktop PC | Micro Desktop PC | Slate / Ultra book | Tablet PC
---|---|---|---
Note / Netbook PC

SOIC | QFP | PBGA | MLF
QFP | PBGA | POP
40 LD SOIC | 38 x 28 | 38 x 28
18 x 28 | 30 x 20 mm | 203 A
1.6 mm | 6.6 mm | 10.5 mm
2.0 mm | 2.0 mm | 2.0 mm

WLFO | WLCSP | FCBGA
WLCSP | POP | CABGA
12 x 12 | 30 x 30 mm | 3.2 mm
3.2 mm | 3.2 mm | 3.2 mm
1.5 mm | 1.5 mm | 1.5 mm
Memory Technology Change

Form Factor

<table>
<thead>
<tr>
<th>Die</th>
<th>2010</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>Total 5.3B units</td>
<td>Total 9.0B units</td>
</tr>
<tr>
<td>8</td>
<td>4 die LGA</td>
<td>8+1 die LGA &amp; BGA</td>
</tr>
<tr>
<td>4</td>
<td>Thin thickness</td>
<td>Thin thickness</td>
</tr>
<tr>
<td>2</td>
<td>Thin thickness</td>
<td>Thin thickness</td>
</tr>
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</table>

Bandwidth Extension

<table>
<thead>
<tr>
<th>8+8 die PoP</th>
<th>16die TSV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thin thickness</td>
<td>Thin thickness</td>
</tr>
</tbody>
</table>

High I/O, Thinner

Prismark 2011

Total 5.3B units

Total 9.0B units
3D Packaging Paradigm Shift

Package Stacking

Package-on-Package

Flip chip + Wire bonding

3D Stacking

Wire bonding + Wire bonding

3D IC

TSV

Package-in-Package

Amkor Proprietary Business Information
Flip Chip / Wire bonding stack

...Evolves into 3D TSV
High End fcBGA

...Evolves into 2.5D TSV

Logic with Embedded memory

Logic and Memory in same Substrate

Logic and Memory with separated
3D TSV Key Process

Foundry / IDM / OSAT

TSV Wafer Processing

Front Side Wafer Finish
(uBump)

Back Side Wafer Finish
(Via reveal/ Passivation/ Plating & etc.)

Assembly
(TSV Die tacking)

Front Micro Bump Pad (Ni/Au)

Temporary bond

Wafer thinning

Flat reveal

Silicon Recess

Bumping

Secondary reveal

Backside passivation

Organic Version

Inorganic Version

Substrate
Chip on Interposer First Process

1st step - CoW Process

Interposer incoming inspection

Top die attach w/ TC or MR

Bake

u-bump underfill

Cure

2nd step - MEOL

Wafer mold

Mold grinding

BS-WBG

BS-Si etch

BS-CVD

BS-CMP

BS-C4 bumping

3rd step - CoS & back end

Wafer saw

CoS w/ MR or TC

(Wafer sawing)

CoS

(CoS)

C4 underfill

Cure

Lid attach

Ball attach

(Mold)

(Mold side grinding)

(MEOl w/o WSS)
Chip on Interposer First Process

1. Front Micro Bump Pad (Ni/Au)
2. Chip Attach & CUF
3. Wafer Mold
4. Organic Version
   - Wafer thinning
   - Flat reveal
   - Cu reveal
   - By WBG+CMP
5. Silicon Recess
   - Dry etch: CF4
6. Backside passivation
   - Pass. coat
7. Secondary reveal
   - Pass. exposure, Develop and cure
   - UBM + C4 plating
8. Inorganic Version
   - C4 Bumping
   - UBM + C4 plating
9. Mold thinning
10. Dicing
Chip Attach to Substrate
Chip on Interposer First Process – High Level Risk

1. Front Micro Bump Pad
   - Ni/Au Pad: Shape, Thickness, IMC embrittlement

2. Chip Attach & CUF: Chip Attach alignment, Flux cleaning, Underfill dispensing

3. Wafer Mold: Warpage, Void

4. Flat Reveal Wafer Thinning + CMP
   - Wafer Cracking, Cu smearing, Cleaning

5. Silicon Recess – Dry Etch (CF4)
   - Cu corrosion, Etch rate variance, Slow Etch, Contaminate

6. Passivation – organic pass. coating, PECVD
   - Wafer Cracking, Edge Arcing, Thickness/Stress control

7. Secondary Reveal – CMP: Wafer Cracking

8. C4 Bumping

9. Mold Thinning (optional)

10. Dicing – Saw street cracking
Chip on Interposer Last Process

**1st step - MEOL**
- Interposer incoming inspection
- WSS bonding
  - BS-WBG
  - BS-Si etch
  - BS-CVD
  - BS-CMP
  - BS-C4 bumping

**2nd step - CoW Process**
- Top die pick & place
  - Mass reflow
  - Underfill
  - Cure
  - Interposer saw w/ carrier
  - De-bonding to mount tape

**3rd step - CoS & back end**
- CoS w/ MR or TC
  - C4 underfill
  - Cure
  - Lid attach
  - Ball attach
Chip on Interposer Last Process

1. Front Micro Bump Pad (Ni/Au)
2. Zone bond

Organic Version
3. Wafer thinning
   Flat reveal
   Cu reveal
   By WBG+CMP
4. Silicon Recess
   Dry etch: CF4
   Pass. coat

Inorganic Version
5-1. Backside passivation
5-2. Inorganic passivation
   PECVD SiN + SiO2
6-1. Secondary reveal
   Pass. exposure, Develop and cure
6-2. SiO2 CMP
7. C4 Bumping
   UBM +C4 plating

8. 2nd Carrier Bonding & 1st Carrier De-bonding
9. Chip Attach & CUF
   UBM +C4 plating

2nd Carrier De-bonding, Dicing
Chip on Interposer Last Process – High Level Risk

1. Front Micro Bump Pad
   - Ni/Au Pad: Shape, Thickness, IMC embrittlement

2. Zone Bond: TTV Control

3. Flat Reveal Wafer Thinning + CMP
   - Wafer Cracking, Cu smearing, Cleaning

4. Silicon Recess – Dry Etch (CF4)
   - Cu corrosion, Etch rate variance, Slow Etch, Contaminate

5. Passivation – Organic pass. coating, PECVD
   - Wafer Cracking, Edge Arcing, Thickness/Stress control

6. Secondary Reveal
   - Wafer Cracking

7. C4 Bumping

8. 2nd Carrier Bonding & 1st Carrier De-bondding

9. Chip Attach on Interposer

10. 2nd Carrier de-bonding
FS NiAu – CoC Evaluation

- CoC Evaluation on E-lytic Ni/Au
  - AOI inspection
  - Ni/Au thickness measurements
  - Auger analysis for surface condition
  - Wafer bonding
  - Simulated backside thermal processes
  - Debond
  - AOI Pad inspection for FM
  - Singulate
  - Mass Reflow
  - TC Bond
  - "FA - X-section, EDX line scan, EDX area mapping"
  - TC CoC
  - FA
FS NiAu Plating Evaluation

- Images - Post UBM Etch Process
  - There are no abnormalities
Edge trim & WSS

• **Process validation**
  – For edge trimming to reduce chipping.
  – Optimization of wafer bonding to minimize thickness variance of temporary bonding adhesive.
  – Minimizing wafer crack on debonding process.
  – EAR(Etchng Adhesive Removal) optimization
Overview of ZoneBOND carrier wafer

- **Silane+FC40 (Z1, release zone)**
  - This is anti-sticky zone.

- **Edge zone (Z2, stiction zone)**
  - Edge zone width is approximately 2.5mm.
  - Minimum edge zone width is 1.5 mm.
  - SU8 is used as the edge zone mask.
Zone treated Carrier Preparation (3)

• Drop test to Acetone

– We can confirm that Zone treated carrier wafer(Z1) to acetone.
– Z1 is non stick. The reaction of the material to the wafer is just to make the material chemically bond to the wafer that as a “Silanol condensation reaction”. Once it reacts with the surface, the single molecule layer that’s permanently attached to the carrier acts as a poly tetrafluoroethylene(PTFE) or “Teflon like” coating on the wafer.
ZoneBOND De-bonding

- Edge Zone Release with EZR & EZD module

EZR Module

EZD Module

EZR Module: 300mm wafer mounted on film frame
Failures & Problems Related with ZoneBOND De-Bonding

- Delamination
- Adhesive squeeze out
- Blisters
- Crack at edge zone
- Crack
- Wafer shift
# World Wide Temporary Bonding Methods

<table>
<thead>
<tr>
<th></th>
<th>Thermal</th>
<th>Zone</th>
<th>Laser</th>
<th>Chemical</th>
<th>Wedge</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Machine</strong></td>
<td>EVG, TEL, SUSS</td>
<td>EVG, SUSS</td>
<td>TAZMO, Yushin, SUSS</td>
<td>TOK</td>
<td>SUSS</td>
</tr>
<tr>
<td><strong>Material</strong></td>
<td>BSI, ShinEtsu, Sumitomo</td>
<td>BSI, ShinEtsu, Sumitomo</td>
<td>3M</td>
<td>TOK</td>
<td>TMAT, Dow</td>
</tr>
<tr>
<td><strong>Machine price</strong></td>
<td>Middle</td>
<td>High</td>
<td>Middle</td>
<td>Middle</td>
<td>High</td>
</tr>
<tr>
<td><strong>Material price</strong></td>
<td>High</td>
<td>High</td>
<td>Middle</td>
<td>High</td>
<td>Middle</td>
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<tr>
<td><strong>TTV</strong></td>
<td>Good</td>
<td>Normal</td>
<td>Good</td>
<td>Normal</td>
<td>Normal</td>
</tr>
<tr>
<td><strong>UPH</strong></td>
<td>Middle</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

![Image of equipment and materials]

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**BSI, ShinEtsu, Sumitomo**

**3M, TOK, SUSS, TMAT, Dow**

**SUSS XBC300**

**ZoneBOND™**

**The miracles of science™**

**HD-3007**

**Material made by WACKER**

**Wafer Support System**
<table>
<thead>
<tr>
<th></th>
<th>POR</th>
<th>NEW</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>System</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Bond</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Advantage</td>
<td>- Using the Si carrier</td>
<td>- Using the Si carrier</td>
</tr>
<tr>
<td>Disadvantage</td>
<td>- Long Bonding time</td>
<td>- Application of Zone carrier</td>
</tr>
<tr>
<td><strong>Bump process</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Advantage</td>
<td>- Applicable issue to the Si carrier</td>
<td>- Applicable issue to the Si carrier</td>
</tr>
<tr>
<td>Disadvantage</td>
<td>- Bad thermal stability</td>
<td></td>
</tr>
<tr>
<td><strong>Debond</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Advantage</td>
<td>- No mount tape damage</td>
<td>- Room temperature debond</td>
</tr>
<tr>
<td>Disadvantage</td>
<td>- Need to high temperature process</td>
<td>- Long remove time to edge adhesion</td>
</tr>
</tbody>
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<th>Chemical</th>
<th>Wedge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advantage</td>
<td>- Using the Si carrier</td>
<td>- Using the Si carrier</td>
<td>- Using the UV cure</td>
<td>- Using the Si carrier</td>
</tr>
<tr>
<td>Disadvantage</td>
<td>- Low out gassing</td>
<td>- Double side bond</td>
<td>- Short bonding time</td>
<td>- Development of an active adhesive</td>
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<tr>
<td></td>
<td>- Using the Glass carrier</td>
<td>- Bad to adhesive stability</td>
<td>- Good to adhesive generality</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Bad to adhesive stability</td>
<td>- Bad to adhesive generality</td>
<td>- Using the hole Glass carrier</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- High stability (thermal, chemical)</td>
<td>- Glass chucking</td>
<td>- Coating the top device</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Weak to void</td>
<td>- Weak to void</td>
<td>- High carrier price</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- High stability</td>
<td>- Glass chucking</td>
<td>- Bad thermal stability</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Room temperature debond</td>
<td>- Weak to void</td>
<td>- Process failure by high warp</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- High thermal stability</td>
<td>- Room temperature debond</td>
<td>- High adhesion stability</td>
<td></td>
</tr>
<tr>
<td><strong>Debond</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Room temperature debond</td>
<td>- Carrier remove to short time</td>
<td>- High adhesion stability</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- High thermal stability</td>
<td>- High thermal stability</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>- No mount tape damage</td>
<td>- Need to high temperature process</td>
<td>- Wafer edge damage</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Room temperature debond</td>
<td>- Bump damage</td>
<td>- High machine price</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- High thermal stability</td>
<td>- Thin wafer handling</td>
<td>- High machine price</td>
<td></td>
</tr>
</tbody>
</table>
WBG and Cleaning

• Process validation
  – Soft reveal
    ▪ Minimizing TTV with accurate control.
    ▪ Cleaning improvement after wet polish.
  – Flat process
    ▪ Only grinding of Si layer at WBG tool not to expose Cu.
    ▪ Using CMP tool to expose Cu and post CMP cleaning
Wafer Thinning & Cleaning
Example of Flat process

<Device>
Mean : 50.1 um
Max : 52.7 um
Min : 46.8 um
TTV : 5.9 um
Dry Etch

• Process validation

  – Soft reveal
    ▪ Acceptable etch rate
    ▪ Optimizing etch rate and uniformity with TSV bonded pairs.
    ▪ Finding via height for ISR process sequence.
  – Flat process
    ▪ Very slow etch rate
    ▪ Optimizing etch rate and uniformity with TSV bonded pairs
    ▪ Etch gas mixing evaluation to improve etch rate without Cu corrosion.
Si recess etching : Dry etch
Si recess etching : Dry etch

- Flat process

- Soft reveal process
PECVD

• Process validation
  – Deposition of SiN and SiO2
  – Confirming deposition rate, uniformity, stress and RI.
  – Setting up measurement method using ellipsometer to check single layer, multi layer.
Dielectric deposition: PECVD

- Pumping gap limits conductance
- Extends 360°
- Radially symmetrical pumping
- Large volume pumping gallery
- Uniformity unaffected by pump

**Silicon Nitride**
- \( \text{SiH}_4(g) + \text{NH}_3(g) + \text{N}_2(g) \rightarrow \text{Si}_x\text{N}_y\text{H}_z(s) + \text{H}_2(g) \)

**Silicon Oxide [Silane-based process]**
- \( \text{SiH}_4(g) + 4\text{N}_2\text{O}(g) + \text{N}_2 \text{(g)} \rightarrow \text{SiO}_2(s) + 4\text{N}_2(g) + \text{H}_2 \text{(g)} + \text{O}_2(g) \)

**Silicon Oxide [TEOS-based process]**
- \( \text{Si(OC}_2\text{H}_5)_4(g) + \text{O}_2(g) \rightarrow \text{SiO}_2(s) + \text{byproducts} \)
Dielectric deposition : PECVD

Center  Middle  Edge

Note
- Found no abnormality.
Dielectric deposition: PECVD

Note
• Found no damage.
Dielectric deposition: PECVD

Note
- Found no damage.
Dielectric deposition : PECVD

Note
• Found no damage.
• Process validation

  - Process optimization to find BKM
    - Oxide/Cu polish process for ISR (Inorganic soft reveal)
    - Si/Cu polish process for flat reveal process
    - Slurry evaluation
    - Post CMP cleaning evaluation
Secondary reveal: CMP

- **Product Features**
  - 3 platen – 4 head polisher
  - Multi zone polishing head
  - In-situ process control optimizes productivity and performance
  - High performance Desica Cleaner

- **Process Controls**
  - Real-Time Profile Control (RTPC™)
    - High-resolution eddy-current endpoint for bulk metal polish step
  - FullScan™ Endpoint
    - Laser endpoint for metal film clearing
  - FullVision™ MX Endpoint
    - Broad-band optical endpoint control for remaining dielectric thickness
  - Si EP/ISPC under development

- **Process BKMs**
  - TSV CMP know-how
  - Low cost/high performance process BKMs for various TSV CMP applications

Proven product and industry benchmark CMP tool
>1500 Reflexion/Refelxion LK shipped by 2011
Secondary reveal : CMP

- 1k nitride and 2.8um oxide were deposited on these wafers, pillar height at wafer center and edge post etch are not high enough for CMP to fully exposed copper after pillar planarization and OP with 5k oxide removal on the field.
Secondary reveal: CMP

- Fast and good pillar planarization achieved
- Minimum field oxide loss during pillar planarization
Secondary reveal: CMP

center

middle

edge
Secondary reveal : CMP

center

middle

edge
Secondary reveal : CMP
Post CMP Topography

W15
Wafer Center
Wafer Middle
Wafer Edge

W25
Secondary reveal: CMP
Layer Thickness confirmation after CMP

Patterned Area Next to Via

Open Field Area
Stealth Dicing

• Process validation
  – Performing SD with wafer frame handling.
  – Evaluation of laser transparent tape.
  – Parameter DOE of laser process
  – Study for auto focus through inorganic passivation
Stealth Dicing

Wafer surface flatness comparison

✓ Observed wafer BG tape laminated by manual process

![Graph showing wafer flatness comparison](image)

Max-Min: 31 μm
Max-Min: 6 μm

**Fig. 2 Wafer flatness comparison**

**Result**
Wafer flatness was much improved after optimize tape laminate condition. With improved condition, can expect stable **Auto Focus result**

= stable cutting quality.
Stealth Dicing

- Investigation for too low SFV on SiN layered wafer

✓ Measured SFV on dicer

![Graph showing SFV check result]

**Result**

SFV was very low at all the point on wafer.
It was around “0.1V” at the lowest case.

*SFV is same as quantity of reflected AF laser from wafer surface.
*Enough high SFV (=enough reflectivity) is required to keep good Z-accuracy
Stealth Dicing

Influence of SiN layer on wafer surface

- Simulation result of reflectivity and suspected root cause of too low SFV

\[ T = n \lambda \gg \text{Emphasize each other} \]

\[ T = (n + \frac{1}{4}) \lambda \gg \text{Weaken each other} \]

Fig. 4 Reflectivity of Auto Focus laser on SiN
3D through silicon via (TSV) chips will represent 9% of the total semiconductors value in 2017, hitting almost $40B. Packaging, assembly and test market will reach to $8B, the middle-end wafer processing activity such as TSV etching filling, wiring, bumping, wafer testing and wafer-level assembly will reach to $3.8B.

# 3D_TSV Commercialization Status

Key to 3D commercialization is a cost/performance ratio!

<table>
<thead>
<tr>
<th>Application</th>
<th>Driver</th>
<th>Status</th>
<th>Barrier</th>
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</thead>
<tbody>
<tr>
<td>Image sensors</td>
<td>Performance, Form factor</td>
<td>Production</td>
<td>None</td>
</tr>
<tr>
<td>CPUs + memory</td>
<td>Performance</td>
<td>28nm Si node or beyond</td>
<td>Cost, process, yield, infrastructure</td>
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<tr>
<td>GPUs + memory</td>
<td>Performance</td>
<td>2014</td>
<td>Cost, process, yield, infrastructure</td>
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<tr>
<td>FPGAs</td>
<td>Performance</td>
<td>Production</td>
<td>process, yield, infrastructure</td>
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<tr>
<td>Wide I/O memory with processor</td>
<td>Performance (bandwidth extension, lower power consumption), Form factor</td>
<td>2013</td>
<td>Cost, process, yield, KGD, infrastructure (including business logistics)</td>
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<tr>
<td>Memory (stacked)</td>
<td>Performance, Form factor (z-height)</td>
<td>2013</td>
<td>Cost, process, yield, assembly</td>
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</tbody>
</table>
Package Stack with TMV™ Technology

Via Formed by laser machining
Package Stack with WLFO Technology

- Std WLFO
- MCM WLFO
- 2.5D Sensor
- F2F
- 3D WLFO
Thank you