Xilinx SSI Technology
Concept to Silicon Development Overview

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Agenda

- Economic Drivers and Technical Challenges
- Xilinx SSI Technology, Power, Performance
- SSI Development Overview
- Summary
Market Dynamics

Video Driving Explosive Growth in Traffic
By 2015 2/3 of Mobile Traffic will be Video

Machine to Machine
- Smart Meters, Security Cameras, Health Care, Telematics, etc.

Mobile Data Traffic

2x Bandwidth growth every 3 years at the SAME POWER BUDGET
On Die IOs Not Scaling

Number of I/Os per 1000 logic cells in the largest FPGA in each family

<table>
<thead>
<tr>
<th>Technology</th>
<th>Year</th>
<th>I/Os per 1000 Logic Cells</th>
</tr>
</thead>
<tbody>
<tr>
<td>350nm</td>
<td>1995</td>
<td>364</td>
</tr>
<tr>
<td>250nm</td>
<td>1997</td>
<td>60</td>
</tr>
<tr>
<td>180nm</td>
<td>1999</td>
<td>24</td>
</tr>
<tr>
<td>130nm</td>
<td>2002</td>
<td>12</td>
</tr>
<tr>
<td>90nm</td>
<td>2004</td>
<td>6</td>
</tr>
<tr>
<td>65nm</td>
<td>2006</td>
<td>4</td>
</tr>
<tr>
<td>40nm</td>
<td>2008</td>
<td>2</td>
</tr>
</tbody>
</table>

Logic doubles with Moore’s Law but I/O quantity does not
The Progression of 3D Technology

Goals for 2.5D / 3D

- Connectivity: Break die to die IO bottleneck
- Capacity: Achieve Integration beyond Moore’s Law
- Power: Reduce Total Power
- Heterogeneous SOC’s: Mixed Functions & Processes
Capacity: Beyond Moore's Law

Manufacturability

Time

500k LC

2M LC

2M LC w/ Stacked Silicon Interconnect

1M LC

Multiple Small Die Slices

Greater capacity, faster yield ramp

Reference:
Node N to N+1 ~ 1.5 to 2 years for Xilinx FPGAs
Well published technology boiler plate

Microbumps
- Access to power / ground / IOs
- Access to logic regions

Through-silicon Vias (TSV)
- Only bridge power / ground / IOs to C4 bumps
- Coarse pitch, low density aids manufacturability
- Etch process (not laser drilled)

Passive Silicon Interposer (65nm Generation)
- 4 conventional metal layers connect micro bumps & TSVs
- No transistors means low risk and no TSV induced performance degradation

Side-by-Side Die Layout
- Minimal heat flux issues
- Minimal design tool flow impact

28nm FPGA Slice 28nm FPGA Slice 28nm FPGA Slice 28nm FPGA Slice

Microbumps
Silicon Interposer
Through-Silicon Vias
C4 Bumps

BGA Balls
Cross-section of 28nm FPGA with SSI
Virtex-7 2000T

28nm Active Die + 65 nm Passive Interposer

Interposer /Package Technology

<table>
<thead>
<tr>
<th>Technology</th>
<th>Specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M4</td>
<td>2um pitch 4 4X layers</td>
</tr>
<tr>
<td>TSV</td>
<td>12um diameter &amp; 180um pitch</td>
</tr>
<tr>
<td>Micro-bump</td>
<td>45um pitch</td>
</tr>
<tr>
<td>C4</td>
<td>180um pitch</td>
</tr>
<tr>
<td>Package</td>
<td>6-2-6 Layer, 1.0 mm BGA pitch</td>
</tr>
</tbody>
</table>

Low risk approach to integrate TSV & u-bump
High density micro-bump for ~50K chip-to-chip connections
Better FPGA low-k stress management with silicon interposer

Courtesy of Xilinx, TSMC, Amkor
Heterogeneous FPGAs with SSI
Virtex-7 HT

Top View
- 28G SerDes
- Fabric Interface
- TSVs

Cross Section
- 28G FPGA FPGA FPGA FPGA 28G
- Passive Interposer

- Yield optimized
- Noise isolation
- 28G process optimized for performance
- FPGA process optimized for power

- 2.8Tb/s ~3X Monolithic
- 16 x 28G Transceivers
- 72 x 13G Transceivers
- 650 IO
2.5D Performance vs. Monolithic

Vehicle 1 - Monolithic packaged 28Gbps Serdes

Vehicle 2 - 2.5D packaged 28Gbps Serdes

- Measurements show 2.5D comparable performance to Monolithic die

Diagrams not drawn to scale

Reduced noise and better performance margin with SSI
2.5D / SSI Takeaways

SSI Technology summary

- Capacity beyond Moore’s law, Faster yield curve
- Breaks die to die IO bottleneck
- Heterogeneous SOCs
- Power advantage

- Stepping stone to true 3D
What areas of design validation and sign off are challenging for 3D and why?

– Circuit Design and Schematic capture
– RTL, Physical Design of Top Die and Interposer
– Extraction
– Functional and Physical Verification (LVS, DRC)
– Chip level functional verification
– STA
– IR/EM/SI or other Electrical analysis
– Assembly and Yield (beyond the scope of this presentation)
State of EDA tools

1. Can the analysis be split into hierarchical independent levels?

2. Can the data for analysis be split into hierarchical independent levels
SSI Full chip
Circuit and Physical Design

**Circuit Design and Schematic capture**
- Electrical modeling of Interposer
- Design of driver and receiver
- HSPICE Simulations with process models from multiple process nodes
- Signal Integrity analysis
- ESD considerations

**Physical Design, Extraction and Verification**
- Manual vs. Auto-routed Interposer
- Like Top Die (e.g. all FPGAs) vs. unlike Top die (FPGAs, w/ 28G SerDes)
- Extraction of Interposer layout
- LVS done on each Top die and multiple die together;
- DRC done on Interposer and Top Die separately
Static Timing Analysis

- Black box ILM generated for each die
- Full chip netlist (w/ extracted Interposer) generated using internal scripts
- Special consideration given to the process distribution

**STA**

- **Top-down view**
  - Interposer
  - TSV
  - uBump
- **Die 1**
- **Die 2**
- **Die 3**
EM/IR and Thermal Analysis: Challenges

Accurate EM/IR and thermal analysis is iterative in stacked Die Scenario.

1. **Calculate Power + leakage**
2. **Calculate Per layer IR/thermal generation**
3. **Apply fixes per layer as needed**

EM/IR by budgeting
3D: The next frontier

- Higher performance chip stacked on top
  - Thermal considerations

- Bottom die includes power TSV’s for top die
  - Can be in older, “TSV-friendly” technology

- Floor-planning is critical:
  - Thermal concerns (stacked thermal flux)
  - TSV keep out zones may be required in bottom die
to avoid stress-induced performance impact

Assembly Technology still evolving
Call-to-Action: Develop & Evolve 3D Standards

Design enablement
- Interposer Models
- EDA Tools for 3D development and verification
- Chip-to-chip interface standards

Manufacturing standards
- DFM rules for TSV, microbump
- Materials: TSV, u-bump
- Thermal budget

Test
- Test HW & u-bump probing
- Known-Good-Die method
- Self Test Required (FPGA programmability is an advantage)
Conclusion

Bandwidth, power and cost demands are beginning to present significant challenges for monolithic silicon.

Stacked Silicon Interconnect is a breakthrough!

- Capacity
- Connectivity
- Power, Performance
- Heterogeneous SOCs

SSI technology is the next big step in IC evolution.
Stacked Silicon Interconnect: A World of Difference

Earth
- Area: ~500 Million km²
- Population: ~6.8 Billion People
- Oceans: 5
- Age: 5 Billion Years

Virtex-7 2000T
- Interposer Area: ~775 mm²
- Population: ~6.8 Billion Transistors
- Chips: 5
- Age: 40 weeks

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