Ivybridge Server Architecture: A Converged Server

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Acknowledgments: Entire IVB Server Team

Hotchips 2014
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Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, and virtual machine monitor (VMM). Functionality, performance or other benefits will vary depending on hardware and software configurations. Software applications may not be compatible with all operating systems. Consult your PC manufacturer. For more information, visit http://www.intel.com/go/virtualization

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Ivytown: IvyBridge Server Processor

IvyBridge Server aka. IVT or IVB Server

Launched in August ‘13 and Feb’14 into two different server segments

- Up to 50% higher performance and energy efficiency over prior generation SandyBridge-E5 2Socket
- Up to 100% higher performance of prior generation Westmere-E7 4Socket

Performance results mentioned on this page are from Intel® Xeon® Processor E5 v2 and Intel® Xeon® Processor E7 v2 publications. Legal disclaimers in following pages. Software and workloads used in performance tests may have been optimized for performance only on Intel® microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.
Primary Product Goals

Cover wide spectrum of server portfolio with a converged architecture

Achieve scalable and energy efficient performance

Capitalize on the technology features of the Intel® 22nm process
Covering the Server Space

Server Space

- **E5**: Efficient Computing/Entry Level server WorkStation High-End-Desktops
- **E7**: Expandable / Mission Critical server

Historically supported via 2 product lines and 2 platforms

- Same core, 2 different uncore\(^1\) designs
- E7 typically lagged E5 by ~1year

Challenges

- Overlap across the segment
- Fundamentally different segment requirements

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\(^1\) Full chip is broken into core and uncore domains. Uncore is full chip except the cores.

<table>
<thead>
<tr>
<th></th>
<th>E5</th>
<th>E7</th>
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<tr>
<td>1 socket</td>
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<td>2 sockets</td>
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</tr>
<tr>
<td>4 sockets ring</td>
<td>4 sockets fully connected</td>
<td>8 sockets</td>
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</table>

Supported Glue-less system socket counts
Converged Architecture

• Super set architecture
  • Glue-less 2/4/8 socket + Extensible Network Controller (XNC) support
  • 15 core/cache slices
  • 2 Memory Controllers
    • Both Native and Buffered memory
  • 2 Home Agents
  • 3 QPI links
  • 40 PCIe* Gen3 lanes
  • Advanced RAS

• Configurability
  • Via chops (see next page)
  • Via feature Enabling/Disabling
Converged Architecture (cont.)

• Chop-able blocks
  - Removal of right column
    • Cores/caches + agents on ring
  - Removal of a row of cores/caches
Path to Performance

Core improvement
- 5% increase in general compute IPC
- Specific ISA enhancements

Socket performance features
- Up to 50% increase of cores & threads
- 25% - 50% increase in cache size and bandwidth
- 25% - 130% increase in memory bandwidth
- Efficient core performance scaling

22nm Process node
- Up to 30% system level performance per watt increase\(^1\)
- Higher product frequencies

\(^1\) Please refer to page 21 for details

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IVB Core

Converged Core across Client and Server processors

New for servers
Replaces SandyBridge and Westmere cores
5% general compute IPC increase

Recap of IVB Core Features

• ISA Additions
  • AVX (Advanced Vector eXtension) Float 16 conversion support
    • 16bit FP data support
  • Optimized REP MOVSB/STOSB ¹
  • Fast access of FS & GS base registers for user-threads
  • Intel® Secure Key - ISA Support for DRNG
  • Digital Random Number Generation instruction
  • Intel® OS Guard – Supervisor Mode Execution Protection

• Micro-architectural enhancements
  • MOV elimination², pipelined divider
  • Next Page prefetcher
  • Shift/rotate and split-load features

¹ Repeat Move Byte String, Store Byte String instructions
² Optimization to eliminate MOV pipeline occupancy
Scalable On-die Interconnect

Goal:
- Scalable ring performance
  - Keep latency and area increase in check
  - Improve performance
- 3 virtual rings
  - North/South switches dynamically configure the rings (as shown below)

"Clockwise" Outer Ring

"Counter-clockwise" Outer Ring
Increased Memory Bandwidth and Socket Scalability

Support higher memory speed
• Up to 1867 DDR3 speed

Increased Memory scheduling efficiency
• Single/Dual Home Agent (HA) / Memory Controller (MC) with 4 DDR3 channels
• Deep buffering
  • 2 level tracker in HA
    • Large first level: Pre-allocated 512 entries
    • 128 entry second level
  • Increased Rd & Wr buffer sizes in MC
    • 48 Read Pending Queue entries per channel
    • 32 Write Pending Queue entries per channel
• MC Scheduler optimizations
  • Improved turnaround timings
  • Efficient Rd/Wr transaction mix scheduling
Enable and Improve Buffered Memory Solution for E7

MC supports Scalable Memory Interface Gen2 in addition to DDR3

- Each SMI2 connects to a memory extension buffer (MXB)
- Each memory extension buffer connects to 2 DDR3 channels
- Up to 3 DIMMs per channel support

Two operation modes selectable in BIOS

- High reliability mode: Lock-step channels
  - DDDC support (Dual Device Data Correction)
- Performance mode: Independent channels
  - SDDC support (Single Device Data Correction)
Resulting Memory Performance

**3Read 1Write traffic mix**

- ~10% Bandwidth increase at same DDR3 speed
- ~13% BW increase at 16.7% DDR3 speed increase
- Similar idle / loaded latencies despite core count growth
- ~23% Bandwidth increase at total 16.7% DDR3 speed increase over SNB-EP

**2Socket E5 v2 local memory BW compared to prior generation**

**4Socket E7 v2 local memory BW compared to prior generation**

**Increased Efficiency: Higher memory bandwidth increase compared to memory speed increase**

Intel® Xeon® Processor E5 2697 v2 and Intel® Xeon® Processor E7 4890 v2 memory bandwidth and latency results are compared to prior generation E5 and E7 products.

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Coherence Optimizations

Target to improve scalable system performance

Enabling the “in memory snoop directory” (aka. directory mode) for all systems

- Deprecated early snoop for 2 socket E5 systems
  - Improves load to use latencies for clean memory accesses
  - Removes snoop/snoop response processing from critical path

Going from 1bit to 2bit in memory directory

- Tracks 3 states – Invalid/Shared/Any
  - Eliminated need to snoop for Shared state memory accesses
  - Improves latency for Shared state accesses
  - Reduces snoop traffic
New snoop mode to reduce directory overhead

Opportunistic Snoop Broadcast (OSB)

• Speculative snoop broadcast prior to memory directory lookup
• Ignore snoop responses for Invalid/Shared directory state
• Improves cache latency

Dynamically biased for power and performance

• OSB decision is based on available snoop bandwidth
• Usefulness of OSB is tracked to throttle or increase OSB

Highly Configurable

• Enable/disable for different transaction types
• Adjustable thresholds to vary OSB rates for different transaction types
IO Directory Cache (IODC) to reduce directory overhead

Small cache in Home Agent (HA)

- 128 entries addressed by transaction id
- Used only for remote IO write transactions
- Supported only on glue-less system settings

Functionality

- Entry allocated when the invalidation request (InvI2E) is received for a remote write transaction, along with snoop broadcast issue
- Entry de-allocated when the Write-Back data transaction is received by HA

Saves

- The directory lookup and directory update for remote memory IO writes
Improved IO Performance

Large page support for IO Virtualization

- 2MB and 1GB pages in Vt-d (Intel® Virtualization Technology for Directed I/O )
- Critical for small packet workloads with large working sets

Arbitration optimizations for bandwidth

- Improved back to back scheduling
  - Higher PCIe* Gen3 bandwidth
  - Increase in PCIe* P2P (Peer2Peer) Bandwidth

PCIe* Atomics

- Read-Modify-Write transaction to/from IO

Results have been measured with Intel® Data Plane Development Kit internally and are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance.

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New Process: 22nm Process Technology

Improve power/performance

Power Performance Load-line
Internal loadline benchmarking results

95w SNB vs. 70w IVB
~same performance w/ ~33% less power

95w IVB 10c vs. 130w IVB 12c
up to ~28% more perf @~60% more power

95w SNB vs 95w IVB
up to ~25% more perf @ ~9% less power

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Summary: A well balanced server processor

Converged architecture covering the server space
- Refreshes E5 platforms
- Launches new E7 platforms
- 3 dies, 3 sockets, 75+ SKUs

Focus on balanced and scalable system performance
- New Core and up to 50% more cores at increased frequency
- Up to 50% larger LLC capacity, great LLC throughput
- Major bandwidth improvements to keep the cores “fed”
- Increased CPU/memory frequency AND efficiency
- Improved IO BW

Continued emphasis on power efficiency across the load-line
- With improved performance “when you need it”
- Focus on idle power and peak power/performance efficiency
Backup
References

**Product briefs**

**Data sheets**

**Other manuals and specifications**
- Further product details and performance publications available through [www.intel.com](http://www.intel.com) and [http://ark.intel.com](http://ark.intel.com)
IVB Server products and platforms

E5 platform: Romley
- IVB Server - Romley platform refresh
  - E5 2600 - 1,2,4 sockets glueless and 2 socket scalable systems
  - E5 2400 - 1,2 sockets

E7 platform: Brickland
- New platform
  - 2, 4, 8 sockets glueless and 2, 4 socket scalable systems
IVB Server Products and Platforms

Romley: IVB Refresh Platform: 1, 2, 4 socket (S) glueless

- **E5 v2 2S** w/3 Native DDR3, 20 PCIe lanes, 1 QPI link per socket
- **E5 v2 2S** w/4 Native DDR3, 40 PCIe lanes, 2 QPI links per socket

Brickland: New IVB EX Platform: 2, 4, 8 socket glueless

- **E5 v2 4S** w/4 Native DDR3, 40 PCIe lanes, 2 QPI links per socket
- **E7 v2 4S** w/8 Native DDR3 through Memory eXtension Buffer chips (MXB) 32 PCIe lanes, 3 QPI links per socket
- **E7 v2 8S** processors and QPI link connectivity shown only
Total 3 IVB Server dies supply all IVB Server SKUs

One die for high core count E5 and all E7, one die each for mid and low core count E5 products
## IVB E5 Server Products

Product names and specifications

### 2 Socket SKUs

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<tr>
<th>Product Name</th>
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<th>Last Level Cache Size</th>
<th>TDP Frequency</th>
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IVB E5 Server Products (cont.)

Product names and specifications

4 Socket SKUs

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1 Socket Server, Workstation SKUs

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High End Desktop SKUs not shown. Please refer to [www.intel.com](http://www.intel.com) for further product and SKU information.
## IVB E5 Entry Level Server Products

### Product names and specifications

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#### 1 Socket SKUs

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<th>Max TDP Power</th>
<th>Last Level Cache Size</th>
<th>TDP Frequency</th>
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## IVB E7 Server Products

### Product names and specifications

#### 2, 4 and 8 Socket Scalable SKUs

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