UltraScale+ MPSoC and FPGA Families

Vamsi Boppana, Sagheer Ahmad, Ilya Ganusov, Vinod Kathail
Vidya Rajagopalan, Ralph Wittig

HotChips 27, August 2015
Introducing the XC2064...

The First FPGA (1985)
- 64 flip flops
- 128 3-LUTs
- 58 I/O pins
- 18MHz (toggle)
- 2um 2LM
Since then...

- 10,000x More Logic
  - Plus Embedded IP
    - Memory
    - Microprocessor
    - DSP
    - Gigabit Serial I/O

- 100x Faster
- 5000x Lower Power
- 10,000x Lower Cost

So, what’s the problem?

- What to do with all the functionality possible?
- Need programmability
  - Not just hardware… but software programmability
Enter Zynq 7000-AP SoC (2011)

- **ARM® Cortex® A9 Application Processors**
  - Up to 1GHz
  - Single & Double Floating Point

- **7-Series Programmable Logic**
  - 28K-440K Logic Cells
  - Hard PCIe Gen2x8

- **Integrated Memory Mapped Peripherals**
  - e.g. USB2.0, GigE, SDIO, CAN

- **High Bandwidth Memory & DSP**
  - Internal L1/L2 Cache and OCM
  - DDR3, DDR2, LPDDR2 w/ ECC
  - Up to 2.662 GMACs of DSP perf.

- **Integrated Analog**
  - Dual multi-channel 12-bit ADC
  - Up to 1Msps
  - Temp & Voltage sensors

- **AXI Interconnect**
  - Up to 100Gb of bandwidth
  - Over 3000 interconnects
  - ACP Acceleration Port

- **Runtime SW & Tools**
  - Eclipse-based SDK for profiling and performance analysis
  - Cross-trigger/Heterogeneous Debug, Run-time Libraries
  - Extensive support for OS, RTOS, AMP, Hypervisor
  - PetaLinux for easiest out-of-box development

© Copyright 2015 Xilinx
Next generation challenges

- Power, Performance, Cost drivers
- Power management
- 64bit processing
- Real-time processing
- Video and graphics processing
- Pervasive safety and security
- Higher levels of processor-fabric integration
Introducing the Zynq UltraScale+ MPSoC

**ARM Cortex A53 & R5**
- Application processing subsystem
- Real Time processing subsystem
- Memory subsystem for max performance

**IO, Video, Graphics**
- Next-generation coherent interconnect
- High-speed I/Os (PCIe, USB3, SATA, GbE)
- Graphics and Video Processing Engines

**Advanced Power Mgmt**
- Fine-grained power reduction
- System-level software & run time opt

**Processing System**
- Processing System
- Application Processing
- Real-Time Processing
- Graphics Processing
- Power Management
- Memory
- Safety & Security

**General & High-Speed Connectivity**
- Programmable Logic
- UltraRAM
- Video Codec
- Integrated Blocks (PCIe, S_K, MAC)
- High-Speed Transceivers

**Security & Safety**
- Enhanced Authentication, Encryption, Antitamper and trust
- Safety with industry standards support

**Fabric Acceleration**
- UltraScale+ fabric with time borrow
- FinFET performance and power
- HD UltraRAM, and enhanced DSP

**XCVRs & Protocols**
- Power efficient, 32Gbps
- 100G Ethernet and 150G Interlaken
- PCIe Gen3 & Gen4

**Software & Tools**
- Run Time (Xilinx)
  - Linux (64b)
  - Hypervisor
  - OpenAMP
- Run Time (Ecosystem)
  - FreeRTOS
  - Micrium
  - WindRiver & More
- Tools
  - Xilinx SDK
  - Vivado®
  - SDx environments
Zynq UltraScale+ MPSoC Overview

Heterogeneous Multi-Processing

Processing System (PS)

Application Processing Unit
- ARM® Cortex™-A53
- NEON™ Floating Point Unit
- Memory Management Unit
- Embedded Trace Macrocell
- GIC-400, SCU, CCI/SMMU, 1 MB L2 w/ECC

Graphics Processing Unit
- ARM Mali™-400 MP
- Geometry Processor
- Pixel Processor
- Memory Management Unit
- 64 KB L2 Cache

DDR Controller
- DDR4/3/3L, LPDDR4/3 ECC Support
- 256 KB OCM with ECC

High-Speed Connectivity
- DisplayPort
- USB 3.0
- SATA 3.0
- PCIe Gen2
- PS-GTR

Real-Time Processing Unit
- ARM Cortex™-R5
- Vector Floating Point Unit
- Memory Protection Unit
- GIC

Security
- Config AES Decryption, Authentication, Secure Boot
- TrustZone
- Voltage/Temp Monitor

Platform Management Unit
- Power
- System Management

System Control
- DMA, Timers, WDT, Resets, Clocking, & Debug

General Connectivity
- GigE
- CAN
- UART
- SPI
- Quad SPI NOR
- NAND
- SD/eMMC

Programmable Logic (PL)

Storage & Signal Processing
- Block RAM
- UltraRAM
- DSP

General-purpose I/O
- High-Performance HPIO
- High Density HDOI

High-Speed Connectivity
- GTH
- GTY
- 100G EMAC
- PCIe @ Gen4
- Interlaken

Video Codec
- H.265/H.264
- AMS
Introducing the Zynq UltraScale+ MPSoC

**ARM Cortex** A53 & R5
- Application processing subsystem
- Real Time processing subsystem
- Memory subsystem for max performance

**IO, Video, Graphics**
- Next-generation coherent interconnect
- High-speed I/Os (PCIE, USB3, SATA, GbE)
- Graphics and Video Processing Engines

**Advanced Power Mgmt**
- Fine-grained power reduction
- System-level software & run time opt

**Processing System**

- Application Processing
- Real-Time Processing
- Graphics Processing
- Power Management

**Memory**
- Safety & Security

**General & High-Speed Connectivity**

**Programmable Logic**
- UltraRAM
- AMS

**Video Codec**
- Integrated Blocks (PCIe, 10K, MAC)
- High-Speed Transceivers

**Security & Safety**
- Enhanced Authentication, Encryption, Antitamper and trust
- Safety with industry standards support

**Fabric Acceleration**
- UltraScale+ fabric with time borrow
- FinFET performance and power
- HD UltraRAM, and enhanced DSP

**XCVRs & Protocols**
- Power efficient, 32Gbps
- 100G Ethernet and 150G Interlaken
- PCIe Gen3 & Gen4

**Software & Tools**

**Run Time (Xilinx)**
- Linux (64b)
- Hypervisor
- OpenAMP

**Run Time (Ecosystem)**
- FreeRTOS
- Micrium
- WindRiver & More

**Tools**
- Xilinx SDK
- Vivado®
- SDx environments
Application Processing Subsystem

- Quad Cortex-A53 64-bit CPU
  - 32KB each of L1 I & D$ with ECC/Parity
  - 1 MB L2 Cache with ECC
  - Virtualization Support
  - Crypto instructions support
- IO Coherency with ACP & ACE-Lite
- Full Coherency between APU & PL
- Up to 1.5 GHz Frequency
- Power-gating
  - Per core power-gating
  - L2 power-gating
Real-time Processing Subsystem

- **Dual Core Cortex-R5 RPU**
  - Cortex-R5 Lockstep
  - Single & Double precision FPU
  - 32KB of L1 I & D caches w/ ECC
  - 256KB TCM with ECC

- **OCM (On-Chip-Memory)**
  - 256KB OCM with ECC
  - AXI Exclusive monitor support
  - Can be partitioned between different subsystems

- **Up to 600MHz Frequency**

- **Low power domain**
  - Full power domain completely powered off
  - R5s & USBs power-gate-able
Memory Subsystem

- Six-port DDR Controller
  - Supports exclusive monitors
- 32 or 64-bit DDR with ECC
- DDR3/4 and LPDDR3/4
- Up to 2400Mbps
- QoS support for 3 traffic classes
  - Low latency, Real-time, Best-effort
  - Guaranteed latency for RT
- Memory protection, partitioning, and TrustZone support
  - Using XMPU
Introducing the Zynq UltraScale+ MPSoC

- ARM Cortex A53 & R5
  - Application processing subsystem
  - Real Time processing subsystem
  - Memory subsystem for max performance

- Security & Safety
  - Enhanced Authentication, Encryption, Antitamper and trust
  - Safety with industry standards support

- IO, Video, Graphics
  - Next-generation coherent interconnect
  - High-speed I/Os (PCIE, USB3, SATA, GbE)
  - Graphics and Video Processing Engines

- Advanced Power Mgmt
  - Fine-grained power reduction
  - System-level software & run time opt

- Fabric Acceleration
  - UltraScale+ fabric with time borrow
  - FinFET performance and power
  - HD UltraRAM, and enhanced DSP

- XCVRs & Protocols
  - Power efficient, 32Gbps
  - 100G Ethernet and 150G Interlaken
  - PCIe Gen3 & Gen4

- Processing System
  - Application Processing
  - Real-Time Processing

- Memory
  - Safety & Security

- General & High-Speed Connectivity
  - Power Management

- Programmable Logic
  - UltraRAM
  - AMS

- Software & Tools
  - Run Time (Xilinx)
    - Linux (64b)
    - Hypervisor
    - OpenAMP
  - Run Time (Ecosystem)
    - FreeRTOS
    - Micrium
    - WindRiver & More
  - Tools
    - Xilinx SDK
    - Vivado®
    - SDx environments

- Advanced Power Mgnt
  - Fine-grained power reduction
  - System-level software & run time opt

- System-level software & run time opt
PS ↔ PL “Data Mover” Interfaces

- **PL Master Ports**
  - AFI Master ports
  - PL IO-Coherency via CCI
  - PL virtualization via SMMU

- **PL Slave Ports**
  - PS to PL data movers
  - Memory mapped

- **ACP (Accelerated Coherency Port)**
  - ACP for IO (one-way) coherency

- **ACE (AXI Coherency Extn)**
  - Full coherency between PS & PL

- **Per-Port Bandwidth = 85Gbps**
  - Read+write bandwidth
High Speed I/Os

- **USB2/3**
  - 2 independent controllers
  - OTG, Host, Device

- **SATA3**
  - Up to 2 channels

- **Display Port**
  - 4KP30 support
  - 1-2 lanes

- **PCIe Gen2 Rootport or Endpoint**
  - PCIe Gen3/4 EP also hardened

- **SGMII for GbE**
  - 4 independent GbE controllers

- **Tightly integrated transceivers**
Dedicated Video Processing Engines

*Graphics Processing Unit, Video Codec & DisplayPort*

**Video Codec Unit (VCU)**
- More efficient vs. software implementation
  - Higher display density, faster encoding
  - Lower power consumption
- H.265 (HEVC) 8Kx4K (15 fps) 4Kx2K (60 fps)
- 8 and 10 bit per color component
- I, P, B frame support for highest compression

**DisplayPort**
- Video resolution up to 4Kx2K (30 fps)
- Audio up to 8 channels of 24-bit at up to 192 KHz
- Reducing BOM cost by eliminating display driver

**Graphics Processing Unit (GPU)**
- 3D visual, HMI, instrumentation, waveform display
- 1080p resolution graphics
- Mali-400 MP2 up to 667 MHz frequency
Introducing the Zynq UltraScale+ MPSoC

**ARM Cortex A53 & R5**
- Application processing subsystem
- Real Time processing subsystem
- Memory subsystem for max performance

**IO, Video, Graphics**
- Next-generation coherent interconnect
- High-speed I/Os (PCIE,USB3,SATA,GbE)
- Graphics and Video Processing Engines

**Advanced Power Mgmt**
- Fine-grained power reduction
- System-level software & run time opt

**Processing System**
- Application Processing
- Real-Time Processing
- Graphics Processing
- Memory
- Safety & Security

**General & High-Speed Connectivity**
- UltraRAM
- AMS
- Video Codec
- Integrated Blocks (PCle, SLK, MAC)
- High-Speed Transceivers

**Software & Tools**
- Run Time (Xilinx)
  - Linux (64b)
  - Hypervisor
  - OpenAMP
- Run Time (Ecosystem)
  - FreeRTOS
  - Micrium
  - WindRiver & More
- Tools
  - Xilinx SDK
  - Vivado®
  - SDx environments

**Security & Safety**
- Enhanced Authentication, Encryption, Antitamper and trust
- Safety with industry standards support

**Fabric Acceleration**
- UltraScale+ fabric with time borrow
- FinFET performance and power
- HD UltraRAM, and enhanced DSP

**XCVRs & Protocols**
- Power efficient, 32Gbps
- 100G Ethernet and 150G Interlaken
- PCIe Gen3 & Gen4

**Advanced Power Mgmt**
- Fine-grained power reduction
- System-level software & run time opt

**Software & Tools**
- Run Time (Xilinx)
  - Linux (64b)
  - Hypervisor
  - OpenAMP
- Run Time (Ecosystem)
  - FreeRTOS
  - Micrium
  - WindRiver & More
- Tools
  - Xilinx SDK
  - Vivado®
  - SDx environments

**Security & Safety**
- Enhanced Authentication, Encryption, Antitamper and trust
- Safety with industry standards support

**Fabric Acceleration**
- UltraScale+ fabric with time borrow
- FinFET performance and power
- HD UltraRAM, and enhanced DSP

**XCVRs & Protocols**
- Power efficient, 32Gbps
- 100G Ethernet and 150G Interlaken
- PCIe Gen3 & Gen4
Multiple power domains
- Low Power Domain
- Full Power Domain
- PL Power Domain

Power Gating
- A53 per core
- L2 and OCM RAMs
- GPU, USB
- R5s & TCM
- Video Codec

Sleep Mode
- 35mW sleep mode
- Suspend to DDR with power off

---

© Copyright 2015 Xilinx
Security, Safety & Reliability

Advanced Device-Level Secure Processing
- Information Assurance, Anti-Tamper, Trust
- Multi-layered Authentication for Secure System Boot
- Key Management & Revocation

Architected for Safe Systems
- IEC61508 & ISO26262 Functional Safety Standards
- Redundancy, Diversity and Lock-step
- Layered Partitioning: Core / Infrastructure / Peripherals

Delivering High Reliability
- High Availability Systems
- Error Detection & Handling
- Subsystem Isolation & Protection
Introducing the Zynq UltraScale+ MPSoC

**ARM Cortex A53 & R5**
- Application processing subsystem
- Real Time processing subsystem
- Memory subsystem for max performance

**IO, Video, Graphics**
- Next-generation coherent interconnect
- High-speed I/Os (PCIE,USB3,SATA,GbE)
- Graphics and Video Processing Engines

**Advanced Power Mgmt**
- Fine-grained power reduction
- System-level software & run time opt

**Processing System**
- Application Processing
- Real-Time Processing
- Graphics Processing
- Power Management
- Memory
- Safety & Security

**General & High-Speed Connectivity**

**Programmable Logic**

**Fabric Acceleration**
- UltraScale+ fabric with time borrow
- FinFET performance and power
- HD UltraRAM, and enhanced DSP

**XCVRs & Protocols**
- Power efficient, 32Gbps
- 100G Ethernet and 150G Interlaken
- PCIe Gen3 & Gen4

**Software & Tools**

**Run Time (Xilinx)**
- Linux (64b)
- Hypervisor
- OpenAMP

**Run Time (Ecosystem)**
- FreeRTOS
- Micrium
- WindRiver & More

**Tools**
- Xilinx SDK
- Vivado®
- SDx environments
**Tuned Process for Optimal Performance/Watt**

*Optimal Operating Voltage Selection*

### 3D FinFET

- 3D Gate “wraps” around channel for more surface area, achieving
  - Faster transistor on/off switching speeds for greater performance
  - Lower leakage and operating voltage for lower power

<table>
<thead>
<tr>
<th>Voltage</th>
<th>1V</th>
<th>0.95V</th>
<th>0.85V</th>
<th>0.72V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normalized Fabric Performance</td>
<td>1.0x</td>
<td>1.2x</td>
<td>1.6x</td>
<td>1.2x</td>
</tr>
<tr>
<td>Normalized Total Power</td>
<td>1.0x</td>
<td>0.7x</td>
<td>0.8x</td>
<td>0.5x</td>
</tr>
<tr>
<td>Performance/Watt</td>
<td>1.0x</td>
<td>1.7x</td>
<td>2.0x</td>
<td>2.4x</td>
</tr>
</tbody>
</table>
Time Borrow in the Fabric

- **Time-borrowing concept**
  - Shift available slack from fast stages to performance-critical paths

- **UltraScale+ time-borrowing platform**
  - Fine-grain delays to adjust clock skew
  - Programmable pulse generators for latch-based time borrow

- **High Performance without design changes**
  - Very effective on high-performance designs
  - Transparent to customers, part of default flow

---

Example

<table>
<thead>
<tr>
<th>Example</th>
<th>Tmin</th>
<th>Fmax</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline</td>
<td>2.5 ns</td>
<td>400 MHz</td>
</tr>
<tr>
<td>Time Borrow</td>
<td>2 ns</td>
<td>500 MHz</td>
</tr>
</tbody>
</table>
**Extra Pipeline Analysis in Vivado**

- **New automatic pipeline analysis**
  - Automatically analyses design at any SPR stage
  - Finds sequential loops, analyzes timing
  - Detailed latency vs Fmax analysis

- **Enables rapid design exploration**
  - Shows path to 800MHz+ Fmax
  - Suggests most efficient places to insert regs in RTL

- **Backward-compatible**
  - 7-series, UltraScale, UltraScale+
  - Compatible with HLS and SDAccel/SDSoC

<table>
<thead>
<tr>
<th>Clock</th>
<th>Added Latency</th>
<th>Ideal Fmax (MHz)</th>
<th>Ideal Delay (ns)</th>
<th>Requirement (ns)</th>
<th>WNS (ns)*</th>
<th>Added Pipe Reg</th>
<th>Total Pipe Reg</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYS_CLK</td>
<td>0</td>
<td>349.00</td>
<td>2.87</td>
<td>2.31</td>
<td>-0.56</td>
<td>n/a</td>
<td>0</td>
</tr>
<tr>
<td>SYS_CLK</td>
<td>1</td>
<td>354.69</td>
<td>2.82</td>
<td>2.31</td>
<td>-0.51</td>
<td>7693</td>
<td>7693</td>
</tr>
<tr>
<td>SYS_CLK</td>
<td>2</td>
<td>356.97</td>
<td>2.80</td>
<td>2.31</td>
<td>-0.49</td>
<td>5213</td>
<td>12906</td>
</tr>
<tr>
<td>SYS_CLK</td>
<td>3</td>
<td>364.78</td>
<td>2.74</td>
<td>2.31</td>
<td>-0.43</td>
<td>3613</td>
<td>16519</td>
</tr>
<tr>
<td>SYS_CLK</td>
<td>4</td>
<td>366.12</td>
<td>2.73</td>
<td>2.31</td>
<td>-0.42</td>
<td>7348</td>
<td>23867</td>
</tr>
<tr>
<td>SYS_CLK</td>
<td>5</td>
<td>537.24</td>
<td>1.86</td>
<td>2.31</td>
<td>0.45</td>
<td>20348</td>
<td>44215</td>
</tr>
</tbody>
</table>

© Copyright 2015 Xilinx
UltraRAM: New Memory Technology

Up to 432 Mb to replace external memory for cost, power, performance
Unlocking Performance, Bandwidth, & Integration

Enhanced Fabric with FinFET performance
Up to 128 transceivers at up to 32.75 Gb/s
~12,000 DSP slices running at ~900 MHz
UltraRAM for SRAM device replacement
Introducing the Zynq UltraScale+ MPSoC

**ARM Cortex A53 & R5**
- Application processing subsystem
- Real Time processing subsystem
- Memory subsystem for max performance

**IO, Video, Graphics**
- Next-generation coherent interconnect
- High-speed I/Os (PCIE,USB3,SATA,GbE)
- Graphics and Video Processing Engines

**Advanced Power Mgmt**
- Fine-grained power reduction
- System-level software & run time opt

**Processing System**
- Application Processing
- Graphics Processing
- Memory
- Power Management
- Real-Time Processing
- Safety & Security
- General & High-Speed Connectivity

**Programmable Logic**
- Video Codec
- Integrated Blocks (PCIE, R KN, MAC)
- High-Speed Transceivers

**Security & Safety**
- Enhanced Authentication, Encryption, Antitamper and trust
- Safety with industry standards support

**Fabric Acceleration**
- UltraScale+ fabric with time borrow
- FinFET performance and power
- HD UltraRAM, and enhanced DSP

**XCVRs & Protocols**
- Power efficient, 32Gbps
- 100G Ethernet and 150G Interlaken
- PCIe Gen3 & Gen4

**Software & Tools**
- **Run Time (Xilinx)**
  - Linux (64b)
  - Hypervisor
  - OpenAMP

- **Run Time (Ecosystem)**
  - FreeRTOS
  - Micrium
  - WindRiver & More

- **Tools**
  - Xilinx SDK
  - Vivado®
  - SDx environments

© Copyright 2015 Xilinx
Enhanced transceivers

Diverse, Power Efficient SerDes for Bandwidth

- 16G (GTH) & 32G (GTY) transceivers in PL,
- 6G (GTR) in PS for direct access to key processing elements, with full PHY/IP compliance for key protocols:
  - USB, SATA, DisplayPort, PCIe, Ethernet

Fractional PLLs to Reduce BOM Cost

- Single external oscillator generates GT & logic fabric clocks for multiple non-integer line rates
- Available in GTH, and GTY transceivers
Introducing the Zynq UltraScale+ MPSoC

**ARM Cortex A53 & R5**
- Application processing subsystem
- Real Time processing subsystem
- Memory subsystem for max performance

**IO, Video, Graphics**
- Next-generation coherent interconnect
- High-speed I/Os (PCIE, USB3, SATA, GbE)
- Graphics and Video Processing Engines

**Advanced Power Mgmt**
- Fine-grained power reduction
- System-level software & run time opt

**Security & Safety**
- Enhanced Authentication, Encryption, Antitamper and trust
- Safety with industry standards support

**Fabric Acceleration**
- UltraScale+ fabric with time borrow
- FinFET performance and power
- HD UltraRAM, and enhanced DSP

**XCVRs & Protocols**
- Power efficient, 32Gbps
- 100G Ethernet and 150G Interlaken
- PCIe Gen3 & Gen4

**Processing System**
- Application Processing
- Real-Time Processing
- Power Management
- Memory
- Safety & Security

**General & High-Speed Connectivity**
- Programmable Logic
- UltraRAM
- AMS
- Video Codec
- Integrated Blocks (PCIE, S_KK, MAC)
- High-Speed Transceivers

**Software & Tools**
- **Run Time (Xilinx)**
  - Linux (64b)
  - Hypervisor
  - OpenAMP
- **Run Time (Ecosystem)**
  - FreeRTOS
  - Micrium
  - WindRiver & More
- **Tools**
  - Xilinx SDK
  - Vivado®
  - SDx environments
System Software for MPSoC

- Security Firmware
  - Decryption, authentication, sec. boot
- FSBL, uBoot
- ARM® Trusted Firmware
- Software Test Libraries (BIST)
- Power Management Firmware
  - Granular control of resources
- Inter-Processor Framework - OpenAMP

Processing System

- Application Processing Unit
- Graphics Processing Unit
- Firmware
- Memory
- High-Speed Connectivity

Built in Self-Test Functions (BIST) • Boot
Xilinx SDK
Integrated Environment for Software Design

New & Enhanced Software Tools

- Heterogeneous Multicore Debug
  - Debug & cross triggering for APU/RPU/MicroBlaze™ Processor
- System-level Profiling and Performance Analysis Tools
  - Analysis for interfaces
  - Across processing & Programmable Logic (PL) domains
- Multi-OS Boot Image Tool
  - Creates boot image(s)
  - Supports output from Xilinx & 3rd party IDEs
- System Resource Partitioning Tool
  - Graphic assignment of resources

Industry-standard Tools Support

- Enabling developer-preferred dev /debug environments
Software and Systems running on platforms

Linux CPU Hotplug on REmuS

- REmuS (below) runs Linux, ARM Trusted Firmware, and PMU Firmware
- User uses hotplug interface to power down A53 CPUs

Doom on QEMU and REmuS

- Virtualization Passthrough
  - Linux guest using a GEM
  - SMMU used in QEMU
- XEN tools
  - Built packages with Yocto
  - Integrated into PetaLinux
- ParaVirtual FrameBuffer
  - VNC over PV FrameBuffer
  - DomU runs doom (playable)
SDSoC Development Environment
C/C++ Programming for Zynq SoC and MPSoC

- ASSP-like programming experience
- System-level profiling
- Full system optimizing compiler
- Expert use model for platform developers and system architects

Rapid System Level Performance Estimation

C/C++ Development

System-level Profiling

Specify C/C++ Functions for Acceleration

Full system Optimizing Compiler

ZYNQ SoC

ZYNQ MPSoC
C/C++ application to a complete system using easy-to-use Eclipse IDE

‘One-click’ function acceleration in Programmable Logic

Eliminates manual configuration of SW drivers and HW connectivity

Support for multiple OSes and optimized libraries

Enables reuse of optimized HDL IP Blocks as C-callable libraries
Automated Connectivity Optimization
- Finds the Data Mover and PS-PL interface for optimal dataflow
- Rapid exploration of different system connectivity topologies

Rapid Software Configurable Application Acceleration using C/C++
- Automated function acceleration in programmable logic
- Up to 100X increase in performance vs. software
- System optimized for latency, bandwidth, and hardware utilization
SDSoC: System Level Profiling

- **Rapid system performance estimation**
  - Full system estimation (programmable logic, data communication, processing system)
  - Reports SW/HW cycle level performance and hardware utilization

- **Automated performance measurement**
  - Runtime measurement by instrumentation of cache, memory, and bus utilization
1080p60 Motion Detection using SDSoC

```cpp
main()
get_camera(A);
sobel(A,B);
diff(B,C);
... display(out);
```

Video Platform

C/C++ programming for Zynq – 2 weeks with multiple iterations
Summary

Zynq UltraScale+ MPSoC: 2\textsuperscript{nd} Generation SoC from Xilinx
- Applications processing, Real-time, Graphics, Video, Serial connectivity
- Power management, Safety, Security
- SDSoC: Full system optimizing compiler

More than Moore: Architectural innovation
- 3x CPU performance and 4.5x memory bandwidth (SoC)
- UltraScale+ fabric: 60% higher performance, 2.5x performance/watt (FPGA)
- 3\textsuperscript{rd} generation of silicon interposer technology (3D IC)

Taped out in Jun 2015 on TSMC 16FF+
- Significant power and performance benefits with 3D FinFet transistors
- Diverse SW and systems running on multiple platforms today