Professional H.265/HEVC Encoder LSI Toward High-Quality 4K/8K Broadcast Infrastructure

Code Name: NARA (Next-generation encoder Architecture for Real-time HEVC Application)

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Outline

• Introduction and Background
  • History of NTT’s Video CODEC LSIs
  • Roadmaps toward 4K/8K UHDTV
  • Latest video coding standard (HEVC)
  • Requirements for 4K/8K broadcasting

• NARA Architecture

• NARA Key Features and Functions
  • Single-chip configuration
  • Multi-chip configuration

• NARA Chip Implementation

• Target Applications

• Conclusion
History of NTT’s video CODEC LSIs

Analog Digital

SDTV HDTV

MPEG2 H.264

HDTV UHDTV

H.264 H.265

NHK/NTT-COM Board

MPEG-2/H.264 Transcoder

HDTV H.264 Decoder

ISIL-II ('07) (CoolChips X)

SARA ('07) (HotChips19)

NARA ('15)

HDTV MPEG-2 Encoder

HDTV H.264 Encoder

SARA/D ('08) (CoolChips XI)

HDTV MPEG-2 Decoder

HDTV MPEG-2 Decoder

SuperENCII ('00) (HotChips7)

SuperENC ('98) (HotChips10)

Encoder PCI Board

Encoder PC Card (ICCE2000)

Portable HDTV Encoder (ICCE2001)

NHK/NTT-COM Board

ISIL ('02) (CICC2003)

VASA ('02) (HotChips14)
Roadmap toward 4K/8K UHDTV

- 4K test broadcast over satellite in 2014, 8K in 2016
- 4K/8K commercial broadcast TV programs in 2020
HEVC – High Efficiency Video Coding

- The latest video coding standard (Jan. 2013, Range extensions Apr. 2014)
- Achieves half bit rate compared to H.264, 1/4 to MPEG-2, key technology for 4K/8K

Video coding standards history:

- H.261 (ISDN videophone)
- MPEG-2 (Digital TV, DVD)
- MPEG-4 (Cellular videophone)
- H.264 (Blu-ray, camcorder)
- H.265/HEVC

Year:
- 1990
- 1996
- 1999
- 2003
- 2013
What is HEVC?

- Existing encoding flows, but “adaptive and exhaustive” combination of prediction tools

Video frames → Transform → Quantize → Entropy coding → Encoded stream

![Diagram of HEVC encoding process]

- Inter prediction (motion vector search)
- Intra prediction
- Loop filtering
- Locally decoded frames

Example result:

- H.264: 4x4..32x32 blocks
- HEVC: 33 pred. directions

- Intra (within-a-frame) prediction
- Inter (inter-frame) prediction

*4x4 sub-MB available, but rarely used

Motion Vectors(MV)

Coding Tree Unit(CTU)
(Max. 64x64)
HEVC encoding complexity

- About 30x of MPEG-2 processing time, 5x of H.264 processing time
Requirements for 4K/8K broadcasting

- Practical 4K/8K broadcast infrastructure in 2020
- Latest video coding standard (H.265/HEVC) for high compression
- Color signal robustness against tandem encoding
- High bitrate of up to 600 Mbps

NARA: Professional H.265/HEVC encoder LSI toward high-quality 4K/8K broadcast infrastructure
Main concepts for NARA architecture

• Application specific hardware blocks for processes high computational complexity processes, such as precise motion estimation

• Hierarchical pipeline scheme for decisions on optimal hierarchical coding/prediction/transform unit size with high compression

• Single-chip 4K configuration and multi-chip 8K configuration for practical encoding systems
NARA block diagram

VIF: Video Interface
IFE: Image Feature Extraction
MED: Multi-block-size Edge Detector
IPD: Intra Prediction
WME: Wide-range Motion Estimation
MME: Multi-Block-Size Motion Estimation
IME: Integer pixel Motion Estimation
FME: Fractional pixel Motion Estimation
MC: Motion Compensation
IIM: Intra-Inter Mode Decision
MBUS: Memory BUS
TQ: Transform and Quantization
ITIQ: Inverse Transform and Quantization
DF: Deblocking Filter
SAO: Sample Adaptive Offset filtering
BSO: Bit Stream Out
MUX: Multiplexer
PRISC: Prediction Core RISC
CRISC: Coding Core RISC
MRISC: Middle-level RISC
TRISC: Top-level RISC

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NARA pipeline polices

- Parallel processing for precise motion estimation achieving better coding efficiency
- Strictly sequential calculation (conforming to HEVC standard) desirable for mode decision to precisely evaluate coding bit costs
- Short pipeline stages for efficient rate control
NARA pipeline scheme

- NARA adopts CTU-based hierarchical pipeline scheme
- Filter mode decisions for coding efficiency while keeping image quality:
  - Wide-range ME (WME) -> Multi-block-size ME (MME) -> Integer ME (IME) -> Fractional ME (FME) -> Inter/Intra Mode Decision (IIM)

Pixel data transfer and filtering

Full-tournament mode decision

Block-size-parallel motion search

Squeeze from 4 to 3 sizes by parallel pre-decision
Parallel pre-decision in MME

- Motion estimation for all block sizes by parallel pre-decision
- Filter into three block sizes by parallel pre-decision

WME
MME
IME
Hpel-FME
Qpel-FME
Bipred-FME
IIM
MC
TQ/ITIQ
DF
SAO
CABAC
Block-size parallel motion search in FME

- Motion estimation for 3 block sizes in block-size parallel motion search

WME
MME
IME
Hpel-FME
Qpel-FME
Bipred-FME
IIM
MC
TQ/ITIQ
DF
SAO
CABAC
Full-tournament mode decision in IIM

- Strictly sequential calculation by full-tournament mode decision
- Strictly sequential calculation (conforming to HEVC standard) desirable for mode decision to precisely evaluate of coding bit costs
NARA configurations

- **Capability**
  - Single-chip processing **up to 4K 60fps 4:2:2**
  - Multi-chip scalability **up to 8K 60fps**
Multi-chip configuration

8k
#0
#1
#2
#3

4k

Horizontal split
(Slice or Tile)

Chip #0

Chip #1

Chip #2

Chip #3

Stream of slice/tile #0

Stream of slice/tile #0+#1

Stream of slice/tile #0+#1+#2

Concatenated Stream Out

Host CPU

Reference Image, DF&SAO Image near Slice/Tile Boundaries

Reference Picture Transfer Region

DF&SAO Transfer Region

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Key NARA features and functions

**Single-chip configuration:**

- Complicated HEVC processing mapped to hierarchical pipeline scheme based on coding tree units (CTUs).
- Hierarchical pipeline achieves wide-range motion estimation with $\pm 3847.75 \times \pm 1926.75$ search range and optimized HEVC’s high-precision prediction mode decision.
- 4k/60p 4:2:2 real-time encoding with ultra-low delay for field pickup units (FPUs), high bitrate of up to 600 Mbps for contribution, multi-channel encoding for cloud systems, and multi-standard encoding for smooth migration.

**Multi-chip configuration:**

- Ultra-high definition TV encoded beyond 4K with motion estimation and loop filtering across split boundaries when each chip encodes a partitioned frame.
- Suitable for HEVC-based tandem encoding with 4:2:2 for keeping good color information and two-pass encoding for higher compression of final distribution.
NARA chip implementation
# Physical features

<p>| | |</p>
<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Technology</td>
<td>28nm CMOS</td>
</tr>
<tr>
<td>Number of transistors</td>
<td>83M gates</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>Max 600 MHz</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>Core: 0.9 V</td>
</tr>
<tr>
<td></td>
<td>IO: 1.8/3.3 V</td>
</tr>
<tr>
<td></td>
<td>DDR3: 1.5 V</td>
</tr>
<tr>
<td></td>
<td>PCIe and 3G-SDI: 0.9/1.8 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>Approximately 15.0W</td>
</tr>
<tr>
<td>Package</td>
<td>1152 pin FCBGA (35 x 35mm)</td>
</tr>
<tr>
<td>External memories</td>
<td>DDR3</td>
</tr>
</tbody>
</table>
### Functional features

<table>
<thead>
<tr>
<th>Video</th>
<th>Profile</th>
<th>H.265/HEVC Main, Main 10, Main 4:2:2 10 H.264/AVC Baseline, Main, High, High422</th>
</tr>
</thead>
<tbody>
<tr>
<td>Motion search range</td>
<td>-3847.75/+3847.75 (H) -1926.75/+1926.75 (V)</td>
<td></td>
</tr>
<tr>
<td>Resolution and video</td>
<td>Single-chip: 4096x2160 at up to 60 frames per second Multi-chip: 7860x4320 at up to 60 frames per second</td>
<td>rate</td>
</tr>
<tr>
<td>Others</td>
<td>Audio: Serial I/F x 2 Port</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Stream Out: Parallel x 1 /Serial x 4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PCIe: Gen.2 x 8 Lane</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ethernet: 1000/100/10 Mbps with MAC</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Others: User PES input, STC input/output</td>
<td></td>
</tr>
</tbody>
</table>
Target applications (1)

Digital TV Broadcasting Network Service

- Original
- 3 times encoding and decoding
- 420
- 422
- Embedded CODEC
  Portable Microwave link
- Contribution Transmission
- Satellite
- Edge
- HDTV CODEC
- TV Station
- HDTV CODEC
- TV System
- Distribution Transmission
- Original
- 3 times encoding and decoding
- 420
- 422
- Embedded CODEC
  Portable Microwave link
- Contribution Transmission
- Satellite
- Edge
- HDTV CODEC
- TV Station
- HDTV CODEC
- TV System
- Distribution Transmission
Target applications (2)

- Mobile phones
- Consumer TVs
- Broadcast devices (Cameras, editors, encoders)

4K/8K UHDTV Technology

- Mobile/TV Broadcast $192B
- Advertising $68B
- Cinema $20B
- Medical $21B
- Security/Surveillance $7B
- Industrial Design $17B
- Conferencing/Presentation $7B
- Education/Academic $0.6B

Reference: Interim Report of 4K/8K Roadmap Follow-up Meeting (MIC, Japan) *1USD= 120JPY
Conclusion

- Developed: single-chip 4K 60fps 4:2:2 HEVC video encoder LSI, scalable to 8K 60fps
- 8K scalability achieved inter-chip connectivity and parallel processing functions
- NARA architecture has hierarchical pipeline scheme for CTUs

NARA is a key LSI for professional H.265/HEVC encoder LSI toward high-quality 4K/8K broadcast infrastructure