Helio X20:
The First Tri-Gear Mobile SoC with CorePilot™ 3.0 Technology

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Agenda

**Tri-Gear Concept**

**Challenges**

**Key Technologies**

- Tailored CPU cores for gears
- Enhanced coherent interconnect
- Hybrid scheduler
- Holistic gear allocation
- Adaptive thermal management

**Achievements**

**Summary**
### User Behavior Changed

<table>
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<tr>
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</thead>
<tbody>
<tr>
<td>Web Browsing</td>
<td>Chrome Browser</td>
<td>Heavy ~ Medium</td>
<td>20%</td>
<td>14%</td>
<td>10%</td>
<td>-4%</td>
</tr>
<tr>
<td>Gaming</td>
<td>Temple Run 2</td>
<td>Heavy ~ Light</td>
<td>32%</td>
<td>32%</td>
<td>15%</td>
<td>-17%</td>
</tr>
<tr>
<td>Social Messaging</td>
<td>Facebook</td>
<td>Medium</td>
<td>24%</td>
<td>28%</td>
<td>31%</td>
<td>+3%</td>
</tr>
<tr>
<td>Entertainment, Utilities, and others</td>
<td>YouTube, Mail</td>
<td>Medium ~ Light</td>
<td>24%</td>
<td>26%</td>
<td>44%</td>
<td>+18%</td>
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</tbody>
</table>

- **Social messaging, entertainment, and utilities (with medium to light loads) take up to 75% of user time**

Source: Flurry Analytics
### Task Load Distribution of Scenarios

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Energy Consumption of Scenarios</th>
</tr>
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<tbody>
<tr>
<td>Web Browsing</td>
<td><img src="chart.png" alt="Bar Chart" /></td>
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</tr>
<tr>
<td>Social Messaging</td>
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</tr>
<tr>
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<td><img src="chart.png" alt="Bar Chart" /></td>
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</tbody>
</table>

- **Medium load tasks are important across all scenarios (36% ~ 48%)**
- **Heavy load tasks are still important for specific scenarios**
The Dual-Gear Dilemma

- **Light Tasks**
  - always-on, connected

- **Medium Tasks**
  - game
  - multimedia

- **Heavy Tasks**
The Dual-Gear Dilemma

Execute medium load tasks on

- big → wasted energy
- LITTLE ← cannot meet performance requirement

LITTLE
• always-on, connected

big
• game
• multimedia
The Dual-Gear Dilemma

**Execute medium load tasks on**
- Mid: balance between performance and power

**Light Tasks**
- always-on, connected

**Medium Tasks**
- Sustainable usage
  - game
  - multimedia

**Heavy Tasks**
Introduction to Tri-Gear

1. New **Mid** gear introduced
2. **Min** gear goes for even lower power, **Max** gear aims for higher performance
3. Reduced power consumption across entire performance range
Challenges of Tri-Gear

Evolving to Tri-Gear

- **Revised scheduler**: Balance power and performance between light and heavy tasks.
- **Tailored processors**: Right task to right CPU.
- **Enhanced coherent interconnect**: Control info.
- **Improved thermal sensing, power budgeting**: Maximize thermal performance, prevent overheating.
- **Improved gear management**: Minimize power consumption.
Tri-Gear Concept Challenges

Key Technologies
- Tailored CPU cores for gears
- Enhanced coherent interconnect
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Achievements

Summary
Tailored CPU Cores for Three Gears

Mid gear for efficient performance
- +30% power-efficiency
  - Multi-bit flip-flops optimization
  - Delicate usage of high leakage LVT cells
- +40% performance vs. Min gear
  - LIB and MEM optimizations

Min, Max gears extend power/performance ranges

* Energy and Performance scale relative to the highest point of Min curve
Enhanced Coherent Interconnect

Enhanced from 2 ACE ports to 3 ACE ports

Increased logic → extra power

• ~50% power reduction by sub-module
  Fine-Grain Clock Gating (FGCG)

Coherent Interconnect Power Comparison

- 3-gear
- 2-gear
- 3-gear w/ FGCG

* Power is relative to 2-gear at 1GB/s
Hybrid Scheduler

HMP Dual-Gear scheduler
- Limited to Dual-Gear
- Boot CPU is always on and cannot be migrated (Fixed CPU0)
  
Typically in LITTLE ➔ LITTLE cannot be off

Dual-level HMP scheduler for Tri-Gear?
- Might not be optimal
- Fixed CPU0 limits power saving opportunities

Fixed CPU0

HMP (Heterogeneous Multi-Processing)
SMP (Symmetric Multi-Processing)

Min
Mid
Max
Power-Off
Intelligent Core Activation Technology (ICAT)

ICAT assigns CPU0 dynamically

- Min gear can be off by task migration
- 8%~10% CPU power saved for medium load

Min always online for CPU0 (booted CPU)

ICAT: Min can be offline

* Power is relative to 1 thread with ICAT at 65°C
Asymmetric Multi-Processing (AMP) with ICAT

**AMP**: enhanced HMP with dynamic gear operation for power saving

- Packing tasks to **Mid** for sustainable performance
- Packing tasks to **Min** for low power

**Tri-Gear scheduler**

- **HMP**
- **AMP** (Asymmetric Multi-Processing)

- **SMP**

![Diagram showing AMP and HMP scenarios](image)
Hybrid Scheduler

HMP for high performance
- Instant boost technology
  - Quick response to utilize Max for urgent or heavy tasks

Hybrid = SMP + AMP + HMP
- Inter-gear task migration
  - Dynamic threshold control for energy efficiency and responsiveness
  - Thread-group migration strategy to increase cluster (L2 cache) locality
Enhanced Power Management

Previous Power Management
• Dynamic Voltage & Frequency Scaling (DVFS) and Hot-Plug drivers consider inputs separately:
  • Power budget, performance requests, and system status such as load, Thread Level Parallelism (TLP)
  • Big gear on/off controlled by Hot-Plug driver

Centralized Gear Allocation
• A holistic control to handle increased complexity
• Tracking steady states to avoid unnecessary gear migration overhead
• Linking to user-specified performance, normal, power-saving modes
Adaptive Thermal Management (ATM)

Power budgeting by both core limit and frequency limit for all CPUs

Dual-Gear to Tri-Gear
- More possible solutions from core / frequency combination meeting power target
- 1.5X ~ 3X more possible solutions on core combination alone, depending on TLP

* Power and performance are relative to the highest point of Max curve
* Each point in a curve represents a choice of gear / core / freq
ATM for More Combinations

Previous power allocation
- Simple cost function: power efficiency only
- Large search space: chosen solution might not meet actual system requirement

Precise power allocation
- Comprehensive cost function: power efficiency, system requirement (#core, frequency and power), system overhead
- +10% Performance from considering system requirement
- -5°C max Tj from reducing system overhead: hot-plug vs. DVFS latency

* Power and performance are relative to the highest point of Max curve
* Geekbench v3 Multi-core Performance
Agenda

Tri-Gear Concept

Challenges

Key Technologies
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Achievements

Summary
Energy Saving from Tri-Gear CPU Architecture

Energy saving from Dual-Gear to Tri-Gear

• Up to **-38%** CPU energy measured for scenarios used daily
CorePilot™ Technology Evolvement

### SMP
Symmetric Multi-Processing
- MT6592

### HMP
Heterogeneous Multi-Processing
- MT6595
- Helio P10

### HC
Heterogeneous Computing
- CorePilot™ Technology Evolvement
  - Octa-core with SMP
  - big.LITTLE HMP
  - Global Task Scheduling
- CPU+GPU Computing
- Dynamic Gear Migration for low power
- 12% ~ 38% CPU energy saving

### Tri-Gear
Hybrid Tri-Gear Multi-Processing
- Helio X20
- CorePilot™ Technology Evolvement
  - Tri-Gear CPU Architecture
  - 12% ~ 38% CPU energy saving
Summary

Majority of tasks are medium and light loads
- Added Mid gear and enhanced Min gear

CorePilot™ 3.0 Key Technologies
- Tailored CPU cores for gears
- Enhanced coherent interconnect
- Hybrid scheduler
- Holistic gear allocation
- Adaptive thermal management

Benefit of Tri-Gear
- Up to 38% CPU energy saving for typical scenarios used daily over extended performance range