Samsung Exynos M1 Processor

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M1 Processor

- ISA - ARM v8.0, 64-bit/32-bit compliant.
  - AArch64 (A64), AArch32 (A32 + T32, formerly ARM+Thumb) instruction sets
- Samsung’s first in house, from scratch design.
- 3-year design cycle - Reqs to Tapeout.
- Best in class, quadcore design.
- 2.6Ghz , sub 3-watt/core
- 14nm FinFet
Microarchitecture Overview

• Advanced Branch Prediction
• Quad instruction decode
  – Most instructions map directly to a single uop
• Quad uOP dispatch and retire
• Full Out-of-Order instruction execution
  – Full OoO loads and stores
• Multistride / multistream prefetcher
• Low latency / low power caches
Samsung M1
Micro-Architecture
Branch Prediction:
- Neural Net based predictor
- Two branches/cycle
- Fetch up to 24-bytes/cycle
- 64-entry microBTB
- 4k-entry mainBTB
- 64-entry Call/Return Stack
- Indirect Predictor
- Loop Predictor
- Decoupled AddrQ
Instruction Cache:
- 64kB/4-way
- 128-byte line size
- Read 24-bytes/cycle
- Parity Protected
- Decoupled InstQ
- 256 entry iTLB
Decode / Rename / Retire:
• Decode 4 inst/cycle
• AArch64, AArch32
• Sequencer for multi-uop
• Rename 4-uops/cycle
• Special renaming for FP
• Fast map recovery
• Retire 4-uops/cycle
• 96-entry ROB
• Dispatch 4-uops/cycle
Samsung M1
Micro-Architecture

Integer Execution:
• Issue up to 7 uops/cycle
• 96-entry integer PRF
• 58-entry distributed sched.
• Branch resolution
• ALUC – three source uops
• ALU – two source uops
• Load Address Adder
• Store Address Adder
• Store Data
Floating Point Execution:
- 32-entry scheduler
- 96-entry FP PRF
- FMAC : 5-cycle MAC
  4-cycle Mul
- FADD: 3-cycle

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<th>Operation</th>
<th>Cycle</th>
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<td>FMAC</td>
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<td>FADD</td>
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Load/Store:
- 32kB/8-way Data Cache
- 64-byte line size
- ECC protected
- Out-of-Order loads and stores
- 1-Load/cycle, 4-cycle latency
- 1-Store/cycle
- 8-outstanding misses
- 32-entry dTLB
- 1024-entry L2TLB
- Multi-stride Prefetcher
- Stream/Copy Optimizations
Samsung M1
Micro-Architecture

L2/Biu:
• 2MB, 16-way
• Four banks
• Inclusive w/ filtering
• 22 Cycle latency
• 16-bytes/cycle/CPU
Samsung M1
Basic Pipeline
Samsung M1
Single-core Power and Efficiency

Power (M1/A57)

Efficiency (perf/W)

M1/A57 (M1 @2.3Ghz, A57@2.1Ghz)

Efficiency
Conclusion

• Samsung’s first from scratch CPU design
• Very aggressive, 3-year design schedule
• Cleanly into Production on time
• Performance and efficiency gains over prior generation
• Best in class quad core mobile design
• More to come...