INTRODUCING “PARKER”
Next-Generation Tegra System-On-Chip

Andi Skende | Distinguished Engineer, “Parker” Lead Architect
“PARKER” DESIGN OBJECTIVES

- Deliver the most advanced processor for premium automotive market
  - A deep learning computing platform for autonomous machines
  - Scalable architecture: autopilot to self-driving
  - A single virtualized machine
“PARKER”
NEXT-GENERATION SYSTEM-ON-CHIP

- NVIDIA’s next-generation Pascal graphics architecture
- NVIDIA’s next-generation ARM 64b Denver 2 CPU
- Functional safety for automotive applications
- Hardware-enabled virtualization architecture
- Improvements to SoC architecture to enable modularity and ASIC development efficiency
- Industry-leading 16nm FF process
# Tegra Key Feature Evolution

<table>
<thead>
<tr>
<th></th>
<th>TK1</th>
<th>TX1</th>
<th>“PARKER”</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GPU</strong></td>
<td>Kepler, 192 CUDA cores</td>
<td>Maxwell, 256 CUDA cores</td>
<td>Pascal, 256 CUDA cores 1.5TFlops (fp16)</td>
</tr>
<tr>
<td><strong>CPU</strong></td>
<td>4+1 A15, 2MB+512K L2 ARM v7 32b Or 2 Denver 1, 2MB L2 64b</td>
<td>4x A57 2MB L2 + 4x A53 512KB L2 ARM v8 64b</td>
<td>2x Denver 2 2MB L2 + 4x A57 2MB L2 ARM v8 64b Coherent HMP Architecture</td>
</tr>
<tr>
<td><strong>Camera</strong></td>
<td>4 cameras</td>
<td>6 cameras</td>
<td>Auto HDR 12 cameras</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>64b LPDDR2/3, DDR3L 15 GB/s (LP3, DDR3L)</td>
<td>64b LPDDR4, 25GB/s</td>
<td>128b LPDDR4, ~50 GB/s, ECC</td>
</tr>
<tr>
<td><strong>Display</strong></td>
<td>Dual Pipeline 4K@30fps 24bpp</td>
<td>Dual Pipeline 4K@60fps</td>
<td>Triple Pipeline 4K@60fps</td>
</tr>
</tbody>
</table>
# Tegra Key Feature Evolution

<table>
<thead>
<tr>
<th></th>
<th>TK1</th>
<th>TX1</th>
<th>“PARKER”</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Video</strong></td>
<td>2160P30 decode, 2160P30 encode</td>
<td>2160P60 decode, 2160P30 encode</td>
<td>2160P60 decode, 2160P60 encode</td>
</tr>
<tr>
<td><strong>Storage</strong></td>
<td>e-MMC 4.51, SATA</td>
<td>e-MMC 5.1, SATA</td>
<td>e-MMC 5.2, SATA</td>
</tr>
<tr>
<td><strong>Auto Features</strong></td>
<td>NA</td>
<td>QSPI</td>
<td>Ethernet-AVB, Dual CAN, QSPI</td>
</tr>
<tr>
<td><strong>Resiliency / Safety Features</strong></td>
<td>NA</td>
<td>NA</td>
<td>Automotive rated SoC Extensive set of resiliency features On-die Safety Manager Engine</td>
</tr>
<tr>
<td><strong>Virtualization</strong></td>
<td>NA</td>
<td>NA</td>
<td>HW-assisted Virtualization</td>
</tr>
<tr>
<td><strong>Process</strong></td>
<td>TSMC 28HPM</td>
<td>TSMC 20SOC</td>
<td>TSMC 16FF</td>
</tr>
</tbody>
</table>
“PARKER” CPU COMPLEX

- 2x Denver2 + 4x Cortex-A57
- Fully Coherent HMP system
  - Proprietary Coherent Interconnect
- ARM V8 64-bit
- Highest performance ARM CPU
  - 2nd generation Denver core
  - Significant Perf/W improvements (~30%)
- Dynamic Code Optimization
  - Optimize once, use many times
- 7-wide superscalar
- Low power retention states
“PARKER” CPU PERFORMANCE

SpecInt2K-Rate Relative to “Parker”
**COHERENT HETEROGENEOUS MULTIPROCESSOR**

<table>
<thead>
<tr>
<th></th>
<th>“PARKER” - COHERENT HMP CPU ARCHITECTURE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Heterogeneous</strong></td>
<td>• Schedule the task on the right CPU core</td>
</tr>
<tr>
<td></td>
<td>• Move task/thread to the right core as compute needs change</td>
</tr>
<tr>
<td></td>
<td>• Maximize peak performance and responsiveness</td>
</tr>
<tr>
<td><strong>Coherent</strong></td>
<td>• No software overhead for cache maintenance as the thread moves across clusters</td>
</tr>
<tr>
<td><strong>MultiProcessor</strong></td>
<td>• Great single thread performance</td>
</tr>
<tr>
<td>(Big + Super)</td>
<td>• Maximize aggregate performance</td>
</tr>
<tr>
<td></td>
<td>• Sufficient thread count for automotive and gaming applications</td>
</tr>
</tbody>
</table>
COHERENT HMP - DESIGN CHALLENGES

- Coherency Interconnect
  - Enable coherency across two different micro-architectures (Denver vs. A57)

- Power Management
  - Unified power state and power management architecture across Denver and A57 cores
HW-enabled CPU, GPU and SoC Virtualization

- HW-enabled virtualization
- Up to 8 virtual environments (VMs)
- Virtualization enables integration
  - Example: IVI + IC in one ECU
- Each VM can control its own display pipeline
- Supported by highest quality virtualization software from NVIDIA
VIRTUALIZATION ON “PARKER”

Hardware Features

• ARM CPU virtualization extensions
  • HYP privilege mode for Hypervisor execution
  • vCPU and vGIC state
  • Virtual CPU timer
  • Two-stage MMU translation for access isolation
  • Instruction trapping (e.g. “WFI”)

• System MMU
  • Two-stage address translation
  • Isolation and protection for memory accesses

• Hardware checks
  • Configuration apertures aligned to 64KB
  • Detection of illegal accesses

• GPU
  • Multiple physical channels directly accessible to VMs
  • GPU MMU for isolating many channel contexts
  • Hardware assisted context switching
  • Fine granularity pre-emption for Graphics
  • CUDA compute context preemption at instruction-level boundary

• Audio Processing Engine
  • Per VM Audio DMA channel assignment and isolation

• General Purpose DMA
  • Per VM DMA channel assignment and isolation

• Virtualization aware IO controllers
  • Ethernet-AVB, PCI-E, etc.
“PARKER” - AN AUTOMOTIVE SoC

- Auto Resiliency Features
  - ISO-26262 compliant
  - Extensive support for error detection and correction
  - Safety Engine
    - Dual lock-step RT processor
    - Supports error/fault management and reporting
    - Executes safety diagnostics and recovery libraries
  - In-line DRAM ECC
    - Errors reported to Safety Engine
    - HW-assisted patrol scrubbing and DRAM page blacklisting
  - ECC / parity protection for key on-die memories

- Automotive Centric IO(s)
  - CAN Interface
    - Dual CAN interface
    - Always-ON domain for fast wake-up
      - Conforms to ISO11898-1
      - Time-triggered interface between CAN controllers
  - Ethernet Audio Video Bus
    - Gigabit Ethernet MAC
    - RGMII interface to external PHY or switch
      - Real time bandwidth reservation
“PARKER” AND DRIVE PX 2

12 CPU cores | Pascal GPUs | 8 TFLOPS | 24 DL TOPS

- Scalable
  - Up to two “Parker” chips + two dGPU chips
- Developed as SEooC (Safety-Element-out-of-Context)
  - Provides flexibility to the developers in supporting their specific use cases and safety goals
- Deployed to many OEM and Tier1 partners
  - Supports development of Autonomous Driving solutions

*World’s First AI Supercomputer for Self-Driving Cars*
“PARKER” AND DRIVE PX 2
SUMMARY - TEGRA “PARKER”

• Improved perf/w with Denver 2 CPU core
• Exceptional aggregate (big + super) CPU performance
• Easy of programming through HMP architecture
• Best-in-class integrated GPU core based on the latest Pascal architecture
• A flexible automotive SoC
  • autopilot to self-driving use cases
• The main building component of NVIDIA DRIVE PX 2 platform