POWER9 Processor for the Cognitive Era

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POWER Processor Technology Roadmap

POWER7+ 32 nm
- 2.5x Larger L3 cache
- On-die acceleration
- Zero-power core idle state
- Up to 12 Cores
- SMT 8
- CAPI Acceleration
- High Bandwidth GPU Attach

POWER8 Family 22nm

POWER9 Family 14nm

Built for the Cognitive Era
- Enhanced Core and Chip Architecture Optimized for Emerging Workloads
- Processor Family with Scale-Up and Scale-Out Optimized Silicon
- Premier Platform for Accelerated Computing

1H10
- Enterprise
- 8 Cores
- SMT 4
- eDRAM L3 Cache

2H12

1H14 - 2H16

2H17 - 2H18+

POWER7 45 nm

POWER8 Family 22nm

POWER9 Family 14nm

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2H17 - 2H18+
Emerging Analytics, AI, Cognitive
- New core for stronger thread performance
- Delivers 2x compute resource per socket
- Built for acceleration – OpenPOWER solution enablement

Technical / HPC
- Highest bandwidth GPU attach
- Advanced GPU/CPU interaction and memory sharing
- High bandwidth direct attach memory

Cloud / HSDC
- Power / Packaging / Cost optimizations for a range of platforms
- Superior virtualization features: security, power management, QoS, interrupt
- State of the art IO technology for network and storage performance

Enterprise
- Large, flat, Scale-Up Systems
- Buffered memory for maximum capacity
- Leading RAS
- Improved caching
POWER9 Processor – Common Features

New Core Microarchitecture
- Stronger thread performance
- Efficient agile pipeline
- POWER ISA v3.0

Enhanced Cache Hierarchy
- 120MB NUCA L3 architecture
- 12 x 20-way associative regions
- Advanced replacement policies
- Fed by 7 TB/s on-chip bandwidth

Cloud + Virtualization Innovation
- Quality of service assists
- New interrupt architecture
- Workload optimized frequency
- Hardware enforced trusted execution

Leadership Hardware Acceleration Platform
- Enhanced on-chip acceleration
- Nvidia NVLink 2.0: High bandwidth, advanced new features
- CAPI 2.0: Coherent accelerator and storage attach (PCIe G4)
- New CAPI: Improved latency and bandwidth, open interface

State of the Art I/O Subsystem
- PCIe Gen4 – 48 lanes

High Bandwidth Signaling Technology
- 16 Gb/s interface
  - Local SMP
- 25 Gb/s interface – 25G Link
  - Accelerator, remote SMP

14nm finFET Semiconductor Process
- Improved device performance and reduced energy
- 17 layer metal stack and eDRAM
- 8.0 billion transistors
# POWER9 Processor Family

## Four targeted implementations

**SMP scalability / Memory subsystem**

<table>
<thead>
<tr>
<th>Core Count / Size</th>
<th>SMT4 Core</th>
<th>SMT8 Core</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>24 SMT4 Cores / Chip</td>
<td>12 SMT8 Cores / Chip</td>
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<tr>
<td></td>
<td>Linux Ecosystem Optimized</td>
<td>PowerVM Ecosystem Continuity</td>
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**Scale-Out – 2 Socket Optimized**
- Robust 2 socket SMP system
- Direct Memory Attach
  - Up to 8 DDR4 ports
  - Commodity packaging form factor

**Scale-Up – Multi-Socket Optimized**
- Scalable System Topology / Capacity
  - Large multi-socket
- Buffered Memory Attach
  - 8 Buffered channels

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New POWER9 Cores

Optimized for Stronger Thread Performance and Efficiency

- Increased execution bandwidth efficiency for a range of workloads including commercial, cognitive and analytics
- Sophisticated instruction scheduling and branch prediction for unoptimized applications and interpretive languages
- Adaptive features for improved efficiency and performance especially in lower memory bandwidth systems

Available with SMT8 or SMT4 Cores

8 or 4 threaded core built from modular execution slices

POWER9 SMT8 Core
- PowerVM Ecosystem Continuity
- Strongest Thread
- Optimized for Large Partitions

POWER9 SMT4 Core
- Linux Ecosystem Focus
- Core Count / Socket
- Virtualization Granularity
POWER9 Core Execution Slice Microarchitecture

Re-factored Core Provides Improved Efficiency & Workload Alignment
- Enhanced pipeline efficiency with modular execution and intelligent pipeline control
- Increased pipeline utilization with symmetric data-type engines: Fixed, Float, 128b, SIMD
- Shared compute resource optimizes data-type interchange
Shorter Pipelines with Reduced Disruption

Improved application performance for modern codes
- Shorten fetch to compute by 5 cycles
- Advanced branch prediction

Higher performance and pipeline utilization
- Improved instruction management
  - Removed instruction grouping and reduced cracking
  - Enhanced instruction fusion
  - Complete up to 128 (64 – SMT4 Core) instructions per cycle

Reduced latency and improved scalability
- Local pipe control of load/store operations
  - Improved hazard avoidance
  - Local recycles – reduced hazard disruption
  - Improved lock management
POWER9 – Core Compute

SMT4 Core Resources

Fetch / Branch
- 32kB, 8-way Instruction Cache
- 8 fetch, 6 decode
- 1x branch execution

Slices issue VSU and AGEN
- 4x scalar-64b / 2x vector-128b
- 4x load/store AGEN

Vector Scalar Unit (VSU) Pipes
- 4x ALU + Simple (64b)
- 4x FP + FX-MUL + Complex (64b)
- 2x Permute (128b)
- 2x Quad Fixed (128b)
- 2x Fixed Divide (64b)
- 1x Quad FP & Decimal FP
- 1x Cryptography

Load Store Unit (LSU) Slices
- 32kB, 8-way Data Cache
- Up to 4 DW load or store

Efficient Cores Deliver 2x Compute Resource per Socket
New Instruction Set Architecture Implemented on POWER9

Broader data type support
• 128-bit IEEE 754 Quad-Precision Float – Full width quad-precision for financial and security applications
• Expanded BCD and 128b Decimal Integer – For database and native analytics
• Half-Precision Float Conversion – Optimized for accelerator bandwidth and data exchange

Support Emerging Algorithms
• Enhanced Arithmetic and SIMD
• Random Number Generation Instruction

Accelerate Emerging Workloads
• Memory Atomics – For high scale data-centric applications
• Hardware Assisted Garbage Collection – Optimize response time of interpretive languages

Cloud Optimization
• Enhanced Translation Architecture – Optimized for Linux
• New Interrupt Architecture – Automated partition routing for extreme virtualization
• Enhanced Accelerator Virtualization
• Hardware Enforced Trusted Execution

Energy & Frequency Management
• POWER9 Workload Optimized Frequency – Manage energy between threads and cores with reduced wakeup latency
POWER9 – Data Capacity & Throughput

Big Caches for Massively Parallel Compute and Heterogeneous Interaction

L3 Cache: 120 MB Shared Capacity NUCA Cache
- 10 MB Capacity + 512k L2 per SMT8 Core
- Enhanced Replacement with Reuse & Data-Type Awareness
  12 x 20 way associativity

High-Throughput On-Chip Fabric
- Over 7 TB/s On-chip Switch
- Move Data in/out at 256 GB/s per SMT8 Core

Extreme Switching Bandwidth for the Most Demanding Compute and Accelerated Workloads

High-Throughput On-Chip Fabric
- Over 7 TB/s On-chip Switch
- Move Data in/out at 256 GB/s per SMT8 Core

17 Layers of Metal
POWER9 – Dual Memory Subsystems

**Scale Out**

**Direct Attach Memory**

- 8 Direct DDR4 Ports
  - Up to 120 GB/s of sustained bandwidth
  - Low latency access
  - Commodity packaging form factor
  - Adaptive 64B / 128B reads

**Scale Up**

**Buffered Memory**

- 8 Buffered Channels
  - Up to 230GB/s of sustained bandwidth
  - Extreme capacity – up to 8TB / socket
  - Superior RAS with chip kill and lane sparing
  - Compatible with POWER8 system memory
  - Agnostic interface for alternate memory innovations
POWER9 – CPU Core Performance

Socket Performance

Scale-Out configuration @ constant frequency
POWER9 – Premier Acceleration Platform

- **Extreme Processor / Accelerator Bandwidth and Reduced Latency**
- **Coherent Memory and Virtual Addressing Capability for all Accelerators**
- **OpenPOWER Community Enablement – Robust Accelerated Compute Options**

- **State of the Art I/O and Acceleration Attachment Signaling**
  - PCIe Gen 4 x 48 lanes – 192 GB/s duplex bandwidth
  - 25G Link x 48 lanes – 300 GB/s duplex bandwidth

- **Robust Accelerated Compute Options with OPEN standards**
  - On-Chip Acceleration – Gzip x1, 842 Compression x2, AES/SHA x2
  - CAPI 2.0 – 4x bandwidth of POWER8 using PCIe Gen 4
  - NVLink 2.0 – Next generation of GPU/CPU bandwidth and integration
  - New CAPI – High bandwidth, low latency and open interface using 25G Link
POWER9 – Ideal for Acceleration

**Extreme CPU/Accelerator Bandwidth**

- **PCle Gen3 x16**
  - 1x
  - CPU ➔ Accelerator ➔ GPU

- **PCle Gen4 x16**
  - 2x
  - CPU ➔ Accelerator ➔ GPU

- **POWER8 with NVLink 1.0**
  - 5x
  - CPU ➔ NVIDIA GPU ➔ Accelerator ➔ GPU

- **POWER9 with 25G Link**
  - 7-10x
  - CPU ➔ NVIDIA GPU ➔ Accelerator ➔ GPU

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**Increased Performance / Features / Acceleration Opportunity**

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**Seamless CPU/Accelerator Interaction**

- Coherent memory sharing
- Enhanced virtual address translation
- Data interaction with reduced SW & HW overhead

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**Broader Application of Heterogeneous Compute**

- Designed for efficient programming models
- Accelerate complex analytic / cognitive applications
OpenPOWER Foundation

- Accelerating Open Innovation
- Grown from 5 to over 200 members in less than 3 years

POWER9: Engineered for OpenPOWER Application

- Built for a Broad Range of Deployments and Platforms
- Open and Flexible Solutions
- Ideal for Developers
Enhanced Core and Chip Architecture for Emerging Workloads
- New Core Optimized for Emerging Algorithms to Interpret and Reason
- Bandwidth, Scale, and Capacity, to Ingest and Analyze

Processor Family with Scale-Out and Scale-Up Optimized Silicon
- Enabling a Range of Platform Optimizations – from HSDC Clusters to Enterprise Class Systems
- Extreme Virtualization Capabilities for the Cloud

Premier Acceleration Platform
- Heterogeneous Compute Options to Enable New Application Paradigms
- State of the Art I/O
- Engineered to be Open
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