Reconfigure Your RTL with EFLX

Join the SoC Revolution

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Why Put an FPGA in Your SoC?

EFLX = Embedded Flexible Logic

- Reconfigure critical RTL
  - up-to-date protocols, encryption, filters, interfaces, ...
- Reconfigurable accelerators
- Create new architectures!
Highly Efficient Network Enables Embedded FPGA

~2x higher utilization of LUTs/mm²

Compatible with SoC metal stack
Integrate EFLX with I/O, Datapath &/or Processor

1. Connect to RAM and I/O
2. In your datapath
3. On your processor bus
Example: A 128-tap Programmable FIR

Reconfigure parts or all of RTL in EFLX

- Can reconfigure coefficients in EFLX
- EFLX DSP is only 3x larger than ASIC

<table>
<thead>
<tr>
<th>Design</th>
<th>ASIC RTL mapped to ASIC gates</th>
<th>Same RTL in EFLX Logic LUTs</th>
<th>Optimized RTL in EFLX Logic LUTs</th>
<th>Optimized RTL in EFLX DSP LUTs</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUTs</td>
<td>-</td>
<td>31,775</td>
<td>9,839</td>
<td>0</td>
</tr>
<tr>
<td>DSPs</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>64</td>
</tr>
<tr>
<td>2.5K Cores (mm²)</td>
<td>0.16mm²</td>
<td>12 (14.28mm²)</td>
<td>4 (4.76mm²)</td>
<td>2 (2.38mm²)</td>
</tr>
<tr>
<td>Effective area</td>
<td>0.16mm²</td>
<td>14.28mm²</td>
<td>4.65mm²</td>
<td>0.476mm²</td>
</tr>
<tr>
<td>Relative area</td>
<td>1</td>
<td>89</td>
<td>29</td>
<td>3</td>
</tr>
</tbody>
</table>

18b coefficient, 16b datapath

http://t-filter.appspot.com/fir/index.html

Stop by our demo at the booth

(TSMC 28HPM/C)