THE NEW INTEL® XEON® SCALABLE PROCESSOR
(FORMERLY SKYLAKE-SP)

Akhilesh Kumar
Intel Corporation, 2017
Authors: Don Soltis, Irma Esmer, Adi Yoaz, Sailesh Kottapalli
Notices and Disclaimers

This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest forecast, schedule, specifications and roadmaps.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at intel.com, or from the OEM or retailer.

No computer system can be absolutely secure.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit http://www.intel.com/performance.

Optimization Notice: Intel’s compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice.

Tests document performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit http://www.intel.com/performance.

Results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.

Cost reduction scenarios described are intended as examples of how a given Intel-based product, in the specified circumstances and configurations, may affect future costs and provide cost savings. Circumstances will vary. Intel does not guarantee any costs or cost reduction.

Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether referenced data are accurate.

Intel, the Intel logo, Intel Optane and Xeon are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

* Other names and brands may be claimed as the property of others. © 2017 Intel Corporation.
INTEL® XEON® SCALABLE PROCESSORS
THE FOUNDATION OF DATA CENTER INNOVATION

WORKLOAD DRIVEN PERFORMANCE

COMPUTE, STORAGE, NETWORK OPTIMIZED

SIMPLE AND EASY TO DEPLOY

ARCHITECTED FOR EFFICIENT, SECURE, AND AGILE DATA CENTER
Agenda

- Intel® Xeon® Scalable Processor Overview
- Processor Architecture Details
  - Core Architecture
  - Interconnect and Cache Architecture
  - Memory Subsystem
  - IO Subsystem
- Performance Benchmarks
- Wrap UP
Intel® Xeon® Scalable Processor Overview
Re-architected from the ground up

- Skylake core microarchitecture with data center specific enhancements
- Intel® AVX-512 with 32 DP flops per cycle per core
- Datacenter optimized cache hierarchy – 1MB L2 per core, non-inclusive L3
- New mesh interconnect architecture
- Enhanced memory subsystem
- Modular IO with integrated devices
- New Intel® Ultra Path Interconnect (Intel® UPI)
- Intel® Speed Shift Technology
- Security & Virtualization enhancements (MBE, PPK, MPX)
- Optional Integrated Intel® Omni-Path Fabric (Intel® OPA)

### Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Intel® Xeon® Processor E5/E7 v4</th>
<th>Intel® Xeon® Scalable Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Availability</td>
<td>Q2 2016</td>
<td>Q3 2017</td>
</tr>
<tr>
<td>Cores Per Socket</td>
<td>Up to 22 or 24</td>
<td>Up to 28</td>
</tr>
<tr>
<td>Threads Per Socket</td>
<td>Up to 44 or 48 threads</td>
<td>Up to 56 threads</td>
</tr>
<tr>
<td>Last-level Cache (LLC)</td>
<td>Up to 55MB or 60 MB</td>
<td>Up to 38.5 MB (non-inclusive)</td>
</tr>
<tr>
<td>QPI/UPI Speed (GT/s)</td>
<td>2x or 3x QPI channels @ 9.6 GT/s</td>
<td>Up to 3x UPI @ 10.4 GT/s</td>
</tr>
<tr>
<td>PCIe* Lanes/ Controllers</td>
<td>40 / 10 / PCIe* 3.0 (2.5, 5, 8 GT/s)</td>
<td>48 / 12 / PCIe 3.0 (2.5, 5, 8 GT/s)</td>
</tr>
<tr>
<td>Memory Population</td>
<td>4 channels of up to 3 RDIMMs, LRDIMMs, or 3DS LRDIMMs</td>
<td>6 channels of up to 2 RDIMMs, LRDIMMs, or 3DS LRDIMMs</td>
</tr>
<tr>
<td>Max Memory Speed</td>
<td>Up to 2400</td>
<td>Up to 2666</td>
</tr>
<tr>
<td>TDP (W)</td>
<td>55W-145W</td>
<td>70W-205W</td>
</tr>
</tbody>
</table>
Core Microarchitecture Enhancements

- Larger and improved branch predictor, higher throughput decoder, larger window to extract ILP
- Improved scheduler and execution engine, improved throughput and latency of divide/sqrt
- More load/store bandwidth, deeper load/store buffers, improved prefetcher
- **Data center specific enhancements**: Intel® AVX-512 with 2 FMAs per core, larger 1MB L2 cache

**Core Microarchitecture enhanced for Data Center specific applications**
Intel® Advanced Vector Extensions 512 (Intel® AVX-512)

512-bit wide vectors, 32 operand registers, 8 64b mask registers, Embedded broadcast & rounding

INTEL® AVX-512 DELIVERS SIGNIFICANT PERFORMANCE AND EFFICIENCY GAINS

Source as of June 2017: Intel internal measurements. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. Configuration Summary: 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Purley-EP (Lewisburg) (S2600WF) with 384 GB (12x32GB DDR4-2666) Total Memory, Intel S3610 800GB SSD, BIOS: SE5C620.86B.01.00.0471.040720170924, 04/07/2017, RHEL Kernel: 3.10.0-514.16.1.el7.x86_64 x86_64, Benchmark: Intel® Optimized MP LINPACK
New Intel® Mesh Interconnect Architecture

**2016: INTEL® XEON® PROCESSOR E7 V4, 14NM (BROADWELL EX 24-CORE DIE)**

**2017: INTEL® XEON® SCALABLE PROCESSOR, 14NM (SKYLAKE-SP 28-CORE DIE)**

**INTEL® MESH IMPROVES SCALABILITY WITH HIGHER BANDWIDTH AND REDUCED LATENCIES**

New Intel® Xeon® Scalable Processor Family (Skylake-SP) – Hot Chips 2017
Re-Architected L2 & L3 Cache Hierarchy

<table>
<thead>
<tr>
<th>Previous Architectures</th>
<th>Skylake-SP Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shared L3</td>
<td>Shared L3</td>
</tr>
<tr>
<td>2.5MB/core (inclusive)</td>
<td>1.375MB/core (non-inclusive)</td>
</tr>
</tbody>
</table>

- On-chip cache balance shifted from shared-distributed (prior architectures) to private-local (Skylake architecture):
  - Shared-distributed ➔ shared-distributed L3 is primary cache
  - Private-local ➔ private L2 becomes primary cache with shared L3 used as overflow cache

- Shared L3 changed from inclusive to non-inclusive:
  - Inclusive (prior architectures) ➔ L3 has copies of all lines in L2
  - Non-inclusive (Skylake architecture) ➔ lines in L2 may not exist in L3

**SKYLAKE-SP CACHE HIERARCHY ARCHITECTED SPECIFICALLY FOR DATACENTER USE CASE**
Inclusive vs Non-Inclusive L3

1. Memory reads fill directly to the L2, no longer to both the L2 and L3
2. When a L2 line needs to be evicted, both modified and unmodified lines are written back
3. Data shared across cores are copied into the L3 for servicing future L2 misses

Cache hierarchy architected and optimized for data center use cases:
- Virtualized use cases get larger private L2 cache free from interference
- Multithreaded workloads can operate on larger data per thread (due to increased L2 size) and reduce interconnect and L3 activity
Cache Performance

Relative Change in L2 and L3 Misses Per Instruction for SPECint*_rate 2006 from Broadwell-EP to Skylake-SP

- **Relative L2 MPI**
- **Relative L3 MPI**

**Skylake-SP** cache hierarchy significantly reduces L2 misses without increasing L3 misses compared to Broadwell-EP

Source as of June 2017: Intel internal measurements on platform with Xeon Platinum 8180, Turbo enabled, UPI=10.4, SNC1, 6x32GB DDR4-2666 per CPU, 1 DPC, and platform with E5-2699 v4, Turbo enabled, 4x32GB DDR4-2400, RHEL 7.0. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit [http://www.intel.com/performance](http://www.intel.com/performance).
Memory Subsystem

2 Memory Controllers, 3 channels each ➔ total of 6 memory channels

- DDR4 up to 2666, 2 DIMMs per channel
- Support for RDIMM, LRDIMM, and 3DS-LRDIMM
- 1.5TB Max Memory Capacity per Socket (2 DPC with 128GB DIMMs)
- >60% increase in Memory BW per Socket compared to Intel® Xeon® processor E5 v4

Consistent and low access latency to all memory attached to a socket from any core
Several optimizations for lower latency and higher bandwidth efficiency
New memory failure detection and recovery with Adaptive Double Device Data Correction (ADDDC)

SIGNIFICANT MEMORY BANDWIDTH AND CAPACITY IMPROVEMENTS OVER PRIOR GENERATION
Memory Performance
Bandwidth-Latency Profile

Source as of June 2017: Intel internal measurements on platform with Xeon Platinum 8180, Turbo enabled, UPI=10.4, SNC1, 6x32GB DDR4-2400/2666 per CPU, 1 DPC, and platform with E5-2699 v4, Turbo enabled, 4x32GB DDR4-2400, RHEL 7.0. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance

100% local memory read
Sequential address
New Intel® Ultra Path Interconnect (Intel® UPI)

- Intel® Ultra Path Interconnect (Intel® UPI), replacing Intel® QPI
- Faster link with improved bandwidth for a balanced system design
  - Improved messaging efficiency per packet
- 3 UPI option for 2 socket – additional bandwidth for non-NUMA high bandwidth use cases

### Data Rate

<table>
<thead>
<tr>
<th></th>
<th>QPI</th>
<th>UPI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>9.6</td>
<td>10.4</td>
</tr>
</tbody>
</table>

### Data Efficiency

- 4% to 21% (per wire)

---

**INTEL® UPI ENABLES SYSTEM SCALABILITY WITH HIGHER INTER-SOCKET BANDWIDTH**

Source as of June 2017: Intel internal measurements on platform with Xeon Platinum 8180, Turbo enabled, UPI=10.4, 6x32GB DDR4-2666, 1 DPC, and platform with E5-2699 v4, Turbo enabled, 4x32GB DDR4-2400, RHEL 7.0. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit [http://www.intel.com/performance](http://www.intel.com/performance).

New Intel® Xeon® Scalable Processor Family (Skylake-SP) – Hot Chips 2017
Processor Integrated I/O

3 independent pipelines of x16 PCIe* Gen3
- Each x16 can be bifurcated into 2x8, 1x8+2x4, or 4x4 root ports
- New traffic controller pipeline improves over prior design
- Contains VTd (Virtualization Technology for Directed IO) engine to support address translation and interrupt remapping

Non-Transparent Bridging (NTB)
- One NTB per x16 PCIe, which can be configured as 1x8 or 1x4 NTB

Intel® QuickData Technology (CBDMA)
- 2x bandwidth on Mem-Mem copy
- Supports MMIO-Mem copy

Intel® Volume Management Device (VMD)
- One VMD domain per x16 PCIe

**MODULAR IO DESIGN WITH IMPROVED FEATURE SET FOR CONVERGED DATA CENTER**
I/O Performance

>50% aggregate IO bandwidth improvement in line with memory bandwidth increase for a balanced system performance

Source as of June 2017: Intel internal measurements on platform with Xeon Platinum 8180, Turbo enabled, UPI=10.4, SNC1, 6x32GB DDR4-2400/2666 per CPU, 1 DPC, and platform with E5-2699 v4, Turbo enabled, 4x32GB DDR4-2400, RHEL 7.0. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit http://www.intel.com/performance.
PERFORMANCE BENCHMARKS
Generational Performance Gains on 2-Socket Servers with Intel® Xeon® Scalable Processor

Higher is better

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Relative 2S Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>E5-2699 v4 Baseline</td>
<td>1.65</td>
</tr>
<tr>
<td>Brokerage Firm OLTP</td>
<td>1.33</td>
</tr>
<tr>
<td>SPECvirt_sc*2013</td>
<td>1.40</td>
</tr>
<tr>
<td>Two-tier SAP SD* (Linux)</td>
<td>1.44</td>
</tr>
<tr>
<td>General Integer App Throughput</td>
<td>1.53</td>
</tr>
<tr>
<td>Java Business Ops Critical OPS</td>
<td>1.58</td>
</tr>
<tr>
<td>Technical Compute App Throughput</td>
<td>1.65</td>
</tr>
<tr>
<td>Memory Bandwidth</td>
<td>1.65</td>
</tr>
<tr>
<td>OLTP Database Performance</td>
<td>1.73</td>
</tr>
<tr>
<td>HPC – Molecular Dynamics</td>
<td>1.73</td>
</tr>
<tr>
<td>Network L3 Packet Forwarding</td>
<td>1.77</td>
</tr>
<tr>
<td>Black Scholes</td>
<td>1.87</td>
</tr>
<tr>
<td>Intel® Distribution for LINPACK</td>
<td>2.27</td>
</tr>
</tbody>
</table>


Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance Intel does not control or audit the design or implementation of third party benchmark data or Web sites referenced in this document. Intel encourages all of its customers to visit the referenced Web sites or others where similar performance benchmark data are reported and confirm whether the referenced benchmark data are accurate and reflect performance of systems available for purchase. Configuration: see page 31, 32
Performance Gains on Technical Compute Workloads

Results have been estimated based on internal Intel analysis and are provided for informational purposes only. Geomean of Weather Research Forecasting - Conus 12Km, HOMME, LSTCLSDYNA Explicit, INTES PERMAS V16, MILC, GROMACS water 1.5M_pme, VASP_Si256, NAMD stmv, LAMMPS, Amber GB Nucleosome, Binomial option pricing, Black-Scholes, Monte Carlo European options. Any difference in system hardware or software design or configuration may affect actual performance. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance/datacenter.

Configurations: see page 33,34
Machine Learning Inference Throughput on Intel® Xeon® Platinum 8180 Processor

Intel® Xeon® Platinum 8180 Processor Inference throughput over Intel® Xeon® Processor E5-2699 v4

Intel® Xeon® Platinum Processor delivers up to 2.4x higher Inference throughput performance

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit: http://www.intel.com/performance. Source: Intel measured as of June 2017, INFERENCe using FP32. Configuration Details on Slide: 35-36

New Intel® Xeon® Scalable Processor Family (Skylake-SP) – Hot Chips 2017
Machine Learning Training Throughput on Intel® Xeon® Platinum 8180 Processor

Intel® Xeon® Platinum 8180 Processor Training throughput over Intel® Xeon® Processor E5-2699 v4

Intel® Xeon® Platinum Processor delivers up to 2.2x higher Training throughput performance

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit: http://www.intel.com/performance Source: Intel measured as of June 2017. Configuration Details on Slide:35,36
WRAP UP
Intel® Xeon® Scalable Processor Summary

Architectural innovations to unlock data center performance

- **Up to 60% increase** in compute performance per socket with Intel® AVX-512
- **Improved performance and scalability** with Mesh on-chip interconnect
- L2 and L3 cache hierarchy **optimized for data center workloads**
- Improved memory subsystem with **up to 60% higher memory bandwidth**
- Faster and more efficient Intel® UPI interconnect for **improved scalability**
- Improved integrated IO with **up to 50% higher aggregate IO bandwidth**

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to [http://www.intel.com/performance](http://www.intel.com/performance) Intel does not control or audit the design or implementation of third party benchmark data or Web sites referenced in this document.

Intel encourages all of its customers to visit the referenced Web sites or others where similar performance benchmark data are reported and confirm whether the referenced benchmark data are accurate and reflect performance of systems available for purchase. See pages 7, 13, and 16 for supporting performance data and configuration details.
INTEL® XEON® SCALABLE PROCESSOR PLATFORM

The Secure, Agile, Next-Generation Platform for Multi-Cloud Infrastructures

PERVASIVE PERFORMANCE FOR ACTIONABLE INSIGHTS

- Skylake-SP cores
- Intel® AVX-512
- Feeds: Intel® UPI, 6x DDR4, 48x PCIe Gen3, Intel® SSDs
- Integration: Intel® VMD/Omni-Path / Intel® QuickAssist / Intel® Ethernet

END-TO-END SECURITY

- Intel® AVX-512
- Page Protection Key, Mode Based Execution
- Intel® QAT w/ Secure Key Management
- Intel® Trusted Infrastructure
- Intel® Boot Guard

AGILE SERVICE DELIVERY

- Intel® Volume Management Device Technology
- Communication and Storage Acceleration Libraries
- Intel® Run Sure Technology
- OpenStack Software Optimizations

New Intel® Xeon® Scalable Processor Family (Skylake-SP) – Hot Chips 2017
New Intel® Xeon® Scalable Processor Family (Skylake-SP) – Hot Chips 2017

**Platform Topologies**

**2S Configurations**

- SKL
  - DMI
  - LBG

**4S Configurations**

- SKL
  - DMI
  - LBG

**8S Configuration**

- SKL
  - DMI
  - LBG

INTEL® XEON® SCALABLE PROCESSOR SUPPORTS CONFIGURATIONS RANGING FROM 2S-2UPI TO 8S

(2S-2UPI & 2S-3UPI shown)

(4S-2UPI & 4S-3UPI shown)
Cache Performance

Relative Change in L2 and L3 Misses Per Instruction for SPECfp*_rate
2006 from Broadwell-EP to Skylake-SP

- Relative L2 MPI
- Relative L3 MPI

Skylake-SP cache hierarchy significantly reduces L2 misses without increasing L3 misses compared to Broadwell-EP

Source as of June 2017: Intel internal measurements on platform with Xeon Platinum 8180, Turbo enabled, UPI=10.4, SNC1, 6x32GB DDR4-2666 per CPU, 1 DPC, and platform with E5-2699 v4, Turbo enabled, 4x32GB DDR4-2400, RHEL 7.0. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit http://www.intel.com/performance. Copyright © 2017, Intel Corporation.
Cache Performance

Skylake-SP L2 cache latency has increased by 2 cycles for a 4x larger L2.

Skylake-SP achieves good L3 cache latency even with larger core count.

Source as of June 2017: Intel internal measurements on platform with Xeon Platinum 8180, Turbo enabled, SNC1, 6x32GB DDR4-2666 per CPU, 1 DPC, and platform with Intel® Xeon® E5-2699 v4, Turbo enabled, without COD, 4x32GB DDR4-2400, RHEL 7.0. Cache latency measurements were done using Intel® Memory Latency Checker (MLC) tool.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit http://www.intel.com/performance. Copyright © 2017, Intel Corporation.
Intel® Volume Management Device (Intel® VMD)

Intel® VMD is a CPU-integrated device to aggregate NVMe SSDs into a storage volume and enables other storage services such as RAID:

- Intel® VMD is an “integrated end point” that stops OS enumeration of devices under it.
- Intel® VMD maps entire PCIe* trees into its own address space (a domain).
- Intel® VMD driver sets up and manages the domain (enumerate, event/error handling), but out of fast IO path.

**ELIMINATES ADDITIONAL COMPONENTS TO PROVIDE A FULL-FEATURE STORAGE SOLUTION**
Intel® Xeon® Scalable Processor with Integrated Fabric

Single on-package Omni-Path Host Fabric Interface (HFI)
Fabric component interfaces to CPU using x16 PCIe* lanes
Fabric PCIe lanes are additional to the 48 PCIe lanes
Single cable from CPU package connector to QSFP module
Same socket for processors with or without Omni-Path fabric
  ▪ Intel® Xeon® Scalable Processor Platform can be designed to support both processors
  ▪ Platform design requires an expanded keep-out zone and additional board components to accommodate both processors
Configurations: Average Generational Gains on 2S Servers

New Intel® Xeon® Scalable Processor Family (Skylake-SP) – Hot Chips 2017

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance

4. 1.65x Average Performance: Geomean based on Normalized Generational Performance (estimated based on Intel internal testing of OLTP Brokerage, SAP SD 2-Tier, HammerDB, Server-side Java, SPECint_rate_base2006, SPECfp_rate_base2006, Server Virtualization, STREAM triad, LAMMPS, DPDK L3 Packet Forwarding, Black-Scholes, Intel Distribution for LINPACK.
   b) Up to 1.40x on SPECvirt_sc* 2013: Claim based on best-published 2-socket SPECvirt_sc* 2013 result submitted to/published at http://www.spec.org/virt_sc2013/results/res2016q3/virt_sc2013-20160823-00060-perf.html as of 11 July 2017, Score: 2360 @ 137 VMs vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor with 768 GB (24 x 32 GB, 2R x 4) PC4-2666 DDR4 2666MHz RDIMM) Total Memory on SUSE Linux Enterprise Server 12 SP2. Data Source: http://www.spec.org, Benchmark: SPECvirt_sc* 2013, Score: 3323 @ 189 VMs Higher is better
   g) Up to 1.65x on STREAM - triad: 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Grantley-EP (Wellsbury) with 256 GB Total Memory on Red Hat Enterprise Linux® 6.5 kernel 2.6.32-431 using STREAM NTW avx2 measurements. Data Source: Request Number: 1709, Benchmark: STREAM - Triad, Score: 127.7 Higher is better vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Nepon City with 384 GB Total Memory on Red Hat Enterprise Linux® 7.2-kernel 3.10.0-327 using STREAM AVX 512 Binaries. Data Source: Request Number: 2500, Benchmark: STREAM - Triad, Score: 199 Higher is better
Configurations: Average Generational Gains on 2S Servers

h) **Up to 1.73x on HammerDB**: 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Grantley-EP (Wellsburg) with 384 GB Total Memory on Red Hat Enterprise Linux® 7.1 kernel 3.10.0-229 using Oracle 12.1.0.2.0 (including database and grid) with 800 warehouses. HammerDB 2.18. Data Source: Request Number: 1645, Benchmark: HammerDB, Score: 4.13568e+006 Higher is better vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Purley-EP (Lewisburg) with 768 GB Total Memory on Oracle Linux® 7.2 using Oracle 12.1.0.2.0, HammerDB 2.18. Data Source: Request Number: 2510, Benchmark: HammerDB, Score: 7.18049e+006 Higher is better

i) **Up to 1.73x on LAMMPS**: LAMMPS is a classical molecular dynamics code, and an acronym for Large-scale Atomic/Molecular Massively Parallel Simulator. It is used to simulate the movement of atoms to develop better therapeutics, improve alternative energy devices, develop new materials, and more. E5-2697 v4: 2S Intel® Xeon® processor E5-2697 v4, 2.3GHz, 36 cores, Intel® Turbo Boost Technology and Intel® Hyperthreading Technology on, BIOS 86B0271.R00, 8x16GB 2400MHz DDR4, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Gold 6148: 2S Intel® Xeon® Gold 6148 processor, 2.4GHz, 40 cores, Intel® Turbo Boost Technology and Intel® Hyperthreading Technology on, BIOS 86B.01.00.0412.R00, 12x16GB 2666MHz DDR4, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327.

j) **Up to 1.77x on DPDK L3 Packet Forwarding**: E5-2658 v4: 5 x Intel® XL710-QDA2, DPDK 16.04. Benchmark: DPDK l3fwd sample application Score: 158 Gbits/s packet forwarding at 256B packet using cores. Gold 6152: Estimates based on Intel internal testing on Intel Xeon 6152 2.1 GHz, 2x Intel®, FM10420(RRC) Gen Dual Port 100GbE Ethernet controller (100Gbit/card) 2x Intel® XXV710 PCI Express Gen Dual Port 25GbE Ethernet controller (2x25G/card), DPDK 17.02. Score: 281 Gbits/s packet forwarding at 256B packet using cores, IO and memory on a single socket

k) **Up to 1.87x on Black-Scholes**: which is a popular mathematical model used in finance for European option valuation. This is a double precision version. E5-2697 v4: 2S Intel® Xeon® processor CPU E5-2697 v4 , 2.3GHz, 36 cores, turbo and HT on, BIOS 86B0271.R00, 128GB total memory, 8 x16GB 2400 MHz DDR4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Gold 6148: Intel® Xeon® Gold processor 6148@ 2.4GHz, HQOS, 40 cores 150W. QMS1, turbo and HT on, BIOS SE5C620.86B.01.00.0412.020920172159, 192GB total memory, 12 x 16 GB 2666 MHz DDR4 RDIMM, 1 x 800GB INTEL SSD SC2BA80, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327

l) **Up to 2.27x on LINPACK**: 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Grantley-EP (Wellsburg) with 64 GB Total Memory on Red Hat Enterprise Linux® 7.0 kernel 3.10.0-123 using MP_LINPACK 11.3.1 (Composer XE 2016 U1). Data Source: Request Number: 1636, Benchmark: Intel® Distribution of LINPACK, Score: 1446.4 Higher is better vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Wolf Pass SKX with 384 GB Total Memory on Red Hat Enterprise Linux® 7.3 using mp_linpack_2017.1.013. Data Source: Request Number: 3753, Benchmark: Intel® Distribution of LINPACK, Score: 3295.57 Higher is better
Configurations: Technical Compute Workloads

Up to 1.63x Gains based on Geomean of Weather Research Forecasting - Cocos 12Km, HOMME, LSSTCLS-DYNA Explicit, INTES PERMAS V16, MILL, GROMACS water 1.5M_pme, VASPSi256, NAMDstmv, LAMMPS, Amber GB Nucleosome, Binomial option pricing, Black-Scholes, Monte Carlo European options. Results have been estimated based on internal Intel analysis and are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and features. Any change to any of those factors may cause the results to vary.

You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

For more information go to http://www.intel.com/performance/datacenter.

1. PERMAS by INTES is an advanced Finite Element software system that offers a complete range of physical models at high performance, quality, and reliability. It plays a mission-critical role in the design process at customers from automotive, ship design, aerospace, and more. E5-2657 v4: 2S Intel® Xeon® processor E5-2697 v4, 2.3GHz, 16 cores, turbo on, HT off, NUMA on, BIOS 338.R00, 256 GB total memory (8x 32GB w/ 2400 MT/s, DDR4 4 RDIMM), 4x Intel® SSD DC P3600 2 TB in RAID 0 (stripe size 64k), CentOS Linux* release 7.2, kernel 3.10.0-327.13.1.el7.x86_64, Intel® Composer 2015.5.223. INTES PERMAS V16.00. Gold 6148: Intel® Xeon® Gold 6148 processor, 2.4 GHz, 20 cores, turbo on, HT off, NUMA on, BIOS SESC620.86B.01.00.0412.0209201712159, 384 GB total memory (12x 32GB w/ 2400 MT/s, DDR4 4 RDIMM), 3x Intel® SSD DC P3600 2 TB in RAID 0 (stripe size 64k), CentOS® Linux* release 7.3, kernel 3.10.0-514.10.2.el7.x86_64, Intel® Composer 2016.7.235. INTES PERMAS V16.00.

2. LS-DYNA is the leading product in the crash simulation market. It is used by the automobile, aerospace, construction, military, manufacturing, and bioengineering industries in worldwide. Workload: 2M elements Car2car model with 120ms simulation time. LS-DYNA explicit standard benchmarks tested by Intel. March 2017. E5-2697 v4: 2S Intel® Xeon® processor E5-2697 v4, 2.3GHz, 18 cores, turbo and HT on, BIOS SESC60.86B.01.01.0016.033120161139, 128GB total memory, 8 memory channels / 12x16GB / 2400 MT/s / DDR4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux* 7.2 kernel 3.10.0.

3. Binomial option pricing is a lattice-based approach that uses a discrete-time model of the varying price over time of the underlying financial instrument. This is compute bound, double precision workload. FSI Binomial Workload. OS: Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Testing by Intel March 2017. E5-2697 v4: 2S Intel® Xeon® processor CPU E5-2697 v4 , 2.3GHz, 36 cores, turbo and HT on, BIOS 86B0271.R00, 128GB total memory, 8 slots / 16GB / 2400 MT/s / DDR4 4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Gold 6148: Intel® Xeon® Gold 6148 processor, 2.4GHz, 40 cores, turbo and HT on, BIOS 86B01.00.0412.0209201712159, 128GB total memory, 8 slots / 16GB / 2400 MT/s / DDR4 4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327.

4. Monte Carlo is a numerical method that uses statistical sampling techniques to approximate solutions to quantitative problems. In finance, Monte Carlo algorithms are used to evaluate complex instruments, portfolios, and investments. This is compute bound, double precision workload. FSI Monte Carlo workload. OS: Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Testing by Intel March 2017. E5-2697 v4: 2S Intel® Xeon® processor CPU E5-2697 v4 , 2.3GHz, 36 cores, turbo and HT on, BIOS 86B0271.R00, 128GB total memory, 8 slots / 16GB / 2400 MT/s / DDR4 4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Gold 6148: Intel® Xeon® Gold 6148 processor, 2.4GHz, 40 cores, turbo and HT on, BIOS 86B01.00.0412.0209201712159, 128GB total memory, 8 slots / 16GB / 2400 MT/s / DDR4 4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327.

5. Black-Scholes is a popular mathematical model used in finance for European option valuation. This is a double precision version. E5-2697 v4: 2S Intel® Xeon® processor CPU E5-2697 v4 , 2.3GHz, 36 cores, turbo and HT on, BIOS 86B0271.R00, 128GB total memory, 8 slots / 16GB / 2400 MT/s / DDR4 4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Gold 6148: Intel® Xeon® Gold 6148 processor, 2.4GHz, 40 cores, turbo and HT on, BIOS SESC620.86B.01.00.0412.0209201712159, 128GB total memory, 12 slots / 16GB / 2400 MT/s / DDR4 4 RDIMM, 1 x 800GB INTEL SSD SC2BA80, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327.

6. Amber is a suite of programs for classical molecular dynamics and statistical analysis. The main MD program is PMEMD (Particle Mesh Ewald Molecular Dynamics) employs two separate algorithms for implicit- and explicit-solvent dynamics. Here performance for explicit solvent (PME) is presented. Amber: Version 16 with all patches applied at December, 2016. Workloads: PME Cellulose VNE(408K atoms), PME stmv (1M atoms), BMCE (2M atoms), GB Nucleosome (25K), GB Rubisco (75K). No cut-off was used for GB workloads. Compiled with -mcc2_sdp_o -intelmp -openmp,-DMC2 "defined. Tests performed on March 2017. E5-2697 v4: Executed with 36 MPI, 2 OpenMP. 2S Intel® Xeon® processor E5-2697 v4, 2.3GHz, 36 cores, turbo and HT on, BIOS 86B0271.R00, 8x16GB 2400MHz DDR4, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Gold 6148: Executed with 40 MPI and 2 OpenMP. 2S Intel® Xeon® Gold 6148 processor, 2.4GHz, 40 cores, turbo on, HT on, BIOS 86B01.00.0412.R00, 12x16GB 2666MHz DDR, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327.
### Configurations: Technical Compute Workloads

<table>
<thead>
<tr>
<th>Workload</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VASP</strong></td>
<td>Configuration: The Vienna Ab initio Simulation Package (VASP) is a computer program for atomic scale materials modeling and performs electronic structure calculations and quantum-mechanical molecular dynamics from first principles. VASP provides scientists with fast and precise calculation of materials properties covering wide range of MD methods from DFT, DFT-HF to Random-Phase approximation (GW, ACDFDT). Beta VASP, a release candidate for v6.0. Developer branch provided as &quot;Package&quot; included with download: <a href="https://github.com/vasp-dev/vasp-knl">https://github.com/vasp-dev/vasp-knl</a>. AVX512: Intel® Compiler 17.0.1.132, Intel® MPI 2017u1, ELPA 2016.05.004. Optimization Flags: &quot;-O3 -xCORE-AVX512&quot;, AVX2: Intel® Compiler 17.0.1.132, Intel® MPI 2017u1, ELPA 2016.05.004. Optimization Flags: &quot;-O3 -xCORE-AVX2&quot;, E5-2697 v4: 2S Intel® Xeon® processor E5-2697 v4 2.3 GHz, 18 Cores/Socket, 36 Cores, 72 Threads, HT on, turbo off, BIOS 86B0271.R00, 128GB total memory, 2400 MT/s DDR4 RDIMM, Red Hat Enterprise Linux* 7.2 kernel 3.10.0-327. Gold 6148: Dual Socket Intel® Xeon® processor Gold 6148 2.4 GHz, 20 Cores/Socket, 40 Cores, 80 Threads, HT on, turbo off, BIOS 86B.01.00.0412, 192GB total memory, 2666 MT/s DDR4 RDIMM, Red Hat Enterprise Linux* 7.2 kernel 3.10.0-327.</td>
</tr>
</tbody>
</table>
Configuration Details: Machine Learning

Platform: 2S Intel® Xeon® Platinum 8180 CPU @ 2.50GHz (28 cores), HT disabled, turbo disabled, scaling governor set to “performance” via intel_pstate driver, 384GB DDR4-2666 ECC RAM. CentOS Linux release 7.3.1611 (Core), Linux kernel 3.10.0-514.10.2.el7.x86_64. SSD: Intel® SSD DC S3700 Series (800GB, 2.5in SATA 6Gbps, 25nm, MLC).

Performance measured with: Environment variables: KMP_AFFINITY='granularity=fine, compact', OMP_NUM_THREADS=56, CPU Freq set with cpupower frequency-set -d 2.5G -u 3.8G -g performance

Deep Learning Frameworks:

- **Caffe**: [http://github.com/intel/caffe/](http://github.com/intel/caffe/), revision f96b759f71b2281835f690af267158b82b150b5c. Inference measured with “caffe time --forward_only” command, training measured with “caffe time” command. For “ConvNet” topologies, dummy dataset was used. For other topologies, data was stored on local storage and cached in memory before training. Topology specs from [https://github.com/intel/caffe/tree/master/models/intel_optimized_models](https://github.com/intel/caffe/tree/master/models/intel_optimized_models) (GoogLeNet, AlexNet, and ResNet-50), [https://github.com/intel/caffe/tree/master/models/default_vgg_19](https://github.com/intel/caffe/tree/master/models/default_vgg_19) (VGG-19), and [https://github.com/soumith/convnet-benchmarks/tree/master/caffe/imagenet_winners](https://github.com/soumith/convnet-benchmarks/tree/master/caffe/imagenet_winners) (ConvNet benchmarks; files were updated to use newer Caffe prototxt format but are functionally equivalent). Intel C++ compiler ver. 17.0.2 20170213, Intel MKL small libraries version 2018.0.20170425. Caffe run with “numactl -l”.

- **TensorFlow**: [https://github.com/tensorflow/tensorflow](https://github.com/tensorflow/tensorflow), commit id 207203253b6f8ea5e938a512798429f91d5b4e7e. Performance numbers were obtained for three convnet benchmarks: alexnet, googlenetv1, vgg([https://github.com/soumith/convnet-benchmarks/tree/master/tensorflow](https://github.com/soumith/convnet-benchmarks/tree/master/tensorflow)) using dummy data. GCC 4.8.5, Intel MKL small libraries version 2018.0.20170425, interop parallelism threads set to 1 for alexnet, vgg benchmarks, 2 for googlenet benchmarks, intra op parallelism threads set to 56, data format used is NCHW, KMP_BLOCKTIME set to 1 for googlenet and vgg benchmarks, 30 for the alexnet benchmark. Inference measured with --caffe time --forward_only --engine MKL2017option, training measured with --forward_backward_only option.

- **MxNet**: [https://github.com/dmlc/mxnet](https://github.com/dmlc/mxnet), revision 5efd91a71f36feae483ee882b0358c8d46b5a7aa20. Dummy data was used. Inference was measured with “benchmark_score.py”, training was measured with a modified version of benchmark_score.py which also runs backward propagation. Topology specs from [https://github.com/dmlc/mxnet/tree/master/example/image-classification/symbols](https://github.com/dmlc/mxnet/tree/master/example/image-classification/symbols), GCC 4.8.5, Intel MKL small libraries version 2018.0.20170425.

- **Neon**: ZP/MKL CHWN branch commit id:52bd02ac947a2adabb8a227166a7da5d9123b6d. Dummy data was used. The main.py script was used for benchmarking, in mkl mode. ICC version used : 17.0.3 20170404, Intel MKL small libraries version 2018.0.20170425.
Configuration Details: Machine Learning

Platform: 2S Intel® Xeon® CPU E5-2699 v4 @ 2.20GHz (22 cores), HT enabled, turbo disabled, scaling governor set to “performance” via acpi-cpufreq driver, 256GB DDR4-2133 ECC RAM. CentOS Linux release 7.3.1611 (Core), Linux kernel 3.10.0-514.10.2.el7.x86_64. SSD: Intel® SSD DC S3500 Series (480GB, 2.5in SATA 6Gb/s, 20nm, MLC).

Performance measured with: Environment variables: KMP_AFFINITY='granularity=fine, compact,1,0', OMP_NUM_THREADS=44, CPU Freq set with cpufreq driver, 256GB DDR4-2133 ECC RAM. CentOS Linux release 7.3.1611 (Core), Linux kernel 3.10.0-514.10.2.el7.x86_64. SSD: Intel® SSD DC S3500 Series (480GB, 2.5in SATA 6Gb/s, 20nm, MLC).

Deep Learning Frameworks:

- **Caffe** ([http://github.com/intel/caffe/](http://github.com/intel/caffe/)), revision f96b759f71b2281835f690af267158b82b150b5c. Inference measured with “caffe time --forward_only” command, training measured with “caffe time” command. For “ConvNet” topologies, dummy dataset was used. For other topologies, data was stored on local storage and cached in memory before training. Topology specs from [https://github.com/intel/caffe/tree/master/models/intel_optimized_models](https://github.com/intel/caffe/tree/master/models/intel_optimized_models) (GoogLeNet, AlexNet, and ResNet-50), [https://github.com/intel/caffe/tree/master/models/default_vgg_19](https://github.com/intel/caffe/tree/master/models/default_vgg_19) (VGG-19), and [https://github.com/soumith/convnet-benchmarks/tree/master/caffe/imagenet_winners](https://github.com/soumith/convnet-benchmarks/tree/master/caffe/imagenet_winners) (ConvNet benchmarks; files were updated to use newer Caffe prototxt format but are functionally equivalent). GCC 4.8.5, Intel MKL small libraries version 2017.0.2.20170110.

- **TensorFlow** ([https://github.com/tensorflow/tensorflow](https://github.com/tensorflow/tensorflow)), commit id 207203253b6f8ea5e938a512798429f91d5b4e7e. Performance numbers were obtained for three convnet benchmarks: alexnet, googlenetv1, vgg ([https://github.com/soumith/convnet-benchmarks/tree/master/tensorflow](https://github.com/soumith/convnet-benchmarks/tree/master/tensorflow)) using dummy data. GCC 4.8.5, Intel MKL small libraries version 2018.0.20170425, interop parallelism threads set to 1 for alexnet, vgg benchmarks, 2 for googlenet benchmarks, intra op parallelism threads set to 44, data format used is NCHW, KMP_BLOCKTIME set to 1 for googlenet and vgg benchmarks, 30 for the alexnet benchmark. Inference measured with --caffe time --forward_only --engine MKL2017option, training measured with --forward_backward_only option.

- **MxNet** ([https://github.com/dmlc/mxnet/](https://github.com/dmlc/mxnet/)), revision e9f281a27584cdb78db8ce6b66e648b3d3810d37. Dummy data was used. Inference was measured with “benchmark_score.py”, training was measured with a modified version of benchmark_score.py which also runs backward propagation. Topology specs from [https://github.com/dmlc/mxnet/tree/master/example/image-classification/symbols](https://github.com/dmlc/mxnet/tree/master/example/image-classification/symbols). GCC 4.8.5, Intel MKL small libraries version 2017.0.2.20170110.

- **Neon** ZP/MKL_CHWN branch commit id:52bd02acb947a2adabb8a227166a7da5d9132b6d. Dummy data was used. The main.py script was used for benchmarking , in mkl mode. ICC version used : 17.0.3 20170404, Intel MKL small libraries version 2018.0.20170425.