ReX: A dNTSC™ Receiver System-on-Chip

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Dotcast, Inc.
Content

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- dNTSC™ receiver technology
- ReX architecture
- ReX microarchitecture and implementation
- Configurable Stream Processor (CSP)
- Applications of the dNTSC™ technology
- Summary
Datacasting – transfer of data over television

dNTSC™ – technology for datacasting over analog NTSC television:
  - Up to 4.5Mbit/sec per analog TV channel
  - Receivable within TV station’s A-contour at $10^{-8}$ bit error rate
    (example: A-contour in Los Angeles - 1.67 million households)

Obtained FCC license for the deployment of dNTSC™ in June 2002

Technology developed and productized: modulator, receiver, antenna (for indoor reception)

Commercial service based on dNTSC™ technology – the MovieBeam™ Service by Walt Disney Corp., scheduled for deployment later this year
- Visual data is modulated in quadrature with NTSC visual carrier and aural data is negative amplitude modulated on aural carrier - first implementation uses visual carrier, only

- Data inserted coherent with NTSC framing – symbol rate ~613KHz

- Data spectrum is pre-filtered and subcarrier carefully spaced to minimize visual impairment with NTSC television
Receive DSP Architecture

- Downconversion, Decimation, and I/Q split
- Coarse Carrier Recovery
- Algorithm implemented in software
- Video Sync Processing
- Feedforward Automatic Gain Control
- Fine Carrier Recovery
- Data Isolation
- Adaptive Data Equalization, Video Cancellation, and Joint Controller
- Feedback Automatic Gain Control
- Data Framer
- Forward Error Correction
- ReX Receiver Chip

Algorithm implemented in software

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DSP Architectural Features:

- **Visual subcarrier only, 1-3 Mbps, using 4,16,32, 64, or 128 QAM on single subcarrier that is about –26 dB below video (relative to peak of video)**
- **Data spectrum occupies about 1/6 of TV channel, without perceptibly corrupting TV broadcast**
- **Timing recovery, automatic gain control, and data framing derived from visual TV signal**
- **Patent pending adaptive equalization and video cancellation techniques for robust (re)-acquisition in harsh indoor environment**
- **Self-optimizing joint controller (patent pending) for optimum system-level performance is highly programmable with performance-driving features**
- **Field-proven error correction using concatenated Trellis Coded Modulation and a Reed-Solomon block code**
Design Requirements:

- *Functional robustness* – must handle a wide variety of known and less-known phenomena in the field

- *High computational performance* – the dNTSC decoding algorithm alone requires $>15$ billion operations/sec (BOPS)

- *Low cost* – targeted to fit within a budget of a consumer electronics product.
ReX ASIC Architecture

ASIC Design Philosophy:

- Simplicity
- Configurability and Programmability
- Low-risk fabrication technology

Implementation Goal: design a robust and reliable mass production part (on a tight schedule, of course)
System-on-Chip:

- **CPU Subsystem** – system administrative functions: system I/O, system interrupts, selected DSP applications

- **DSP Subsystem** – dNTSC™ decoding algorithm, FEC, general signal processing
# CPU Subsystem:

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Technology</td>
<td>NEC’s CB-10 (0.25 micron, 5 metal layer)</td>
</tr>
<tr>
<td>CPU core</td>
<td>NU85E (NEC)</td>
</tr>
<tr>
<td>System Interface</td>
<td>PCI, I2C, GPIO, MPEG Serial</td>
</tr>
<tr>
<td>Tuner Interface</td>
<td>I2C</td>
</tr>
<tr>
<td>Clock speed</td>
<td>160/80 MHz</td>
</tr>
<tr>
<td>On-chip SRAM</td>
<td>128 KByte</td>
</tr>
<tr>
<td>On-chip ROM</td>
<td>16 KByte</td>
</tr>
<tr>
<td>Instruction/Data Cache</td>
<td>8/4 KByte</td>
</tr>
<tr>
<td>Debug Support</td>
<td>N-Wire/JTAG</td>
</tr>
<tr>
<td>External Memory Support</td>
<td>ROM, FLASH, SRAM</td>
</tr>
<tr>
<td>OS</td>
<td>ThreadX</td>
</tr>
</tbody>
</table>

Note: CPU Subsystem is ~1/3 of the die area
DSP Subsystem:

- Bus-based system - D-bus
- D-bus agents:
  - Dedicated programmable - FIRs, mixers, FEC, etc.
  - Fully programmable –CSP
- Connectivity: D-bus, and dedicated connections

Note: DSP Subsystem is ~2/3 of the die area
Configurable Stream Processor – CSP:

- Proprietary general-purpose DSP core (patent pending) optimized for processing of data streams
  - ISA consists of scalar and vector instructions - implies scalar and vector registers
  - Configurable and programmable hardware buffers
  - Input/output data stream transfer in parallel with pipe accesses
  - Explicit and implicit buffer synchronization mechanisms
CSP Pipe:

- 52 instructions (scalar, vector, bit-wise, push/pop, etc.)
  - 8-stage pipe
  - 3 memory segments:
    - CSEG (code)
    - GDSEG (buffers)
    - LDSEG (data)
  - Configurable buffers - number and size
  - Interrupt support
Programmable Buffers:

Programmable number of buffers - 1 to 16
- Programmable buffer size – 128, 256, 512, 1K locations
- A vector register (or, a vector) is a portion of a buffer – vector length is programmable
- Vectors are accessed via vector instructions
- Implicit process synchronization - vector instruction will not start “on an empty vector”

Input data supplied via DMA input channel

- Coefficients loaded by the master CPU or initialized under CSP program control

Conceptual view of Vector Multiplication

\[ V_2 = V_0 \times V_1 \]

\( i=0\ldots3 \)

(V1 is a constant vector)
CSP Multiprocessing

CSP_1 → CSP_2 → CSP_3 → CSP_4

CSP_5 → CSP_6

DMA → CSP_7

C x V_1

Multiply

DMA → CSP_8

C x V_1 x V_2

Multiply

Write Ptr

Read Ptr

Write Ptr

Read Ptr

Write Ptr

Read Ptr

Write Ptr

Read Ptr

Write Ptr

Read Ptr

Write Ptr

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Read Ptr
Vital statistics:

- 0.25 micron (NEC)
- 5 metal layers
- ~3M gates
- 12.5mm x 12.5mm
- 160MHz max freq
- 352TBGA package
- taped out: 12/02
- productized: 3/03
- in the box: 5/03
- in the field: 7/03
Applications of dNTSC™

ReX-based wireless set-top box
dNTSC™ broadcast pipe delivers over 25GByte of raw media assets per day *per antenna*.

dNTSC™ is piggybacked on the existing TV infrastructure => extremely low cost distribution channel
dNTSC™ – technology for datacasting over analog NTSC television supporting up to 4.5Mbit/sec @ 10⁻⁸ BER within TV station’s A contour

ReX – first ASIC implementation of the dNTSC™ receiver technology supporting up to 3Mbit/sec over visual subcarrier

dNTSC™ decoding algorithm implemented in ReX as a combination of dedicated- and fully-programmable processing elements (CSPs)

Configurable Stream Processor (CSP) – general-purpose DSP core optimized for stream processing applications

ReX productized and will be used in a consumer device scheduled for commercial deployment in 2003 – Disney’s MovieBeam™ Service
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